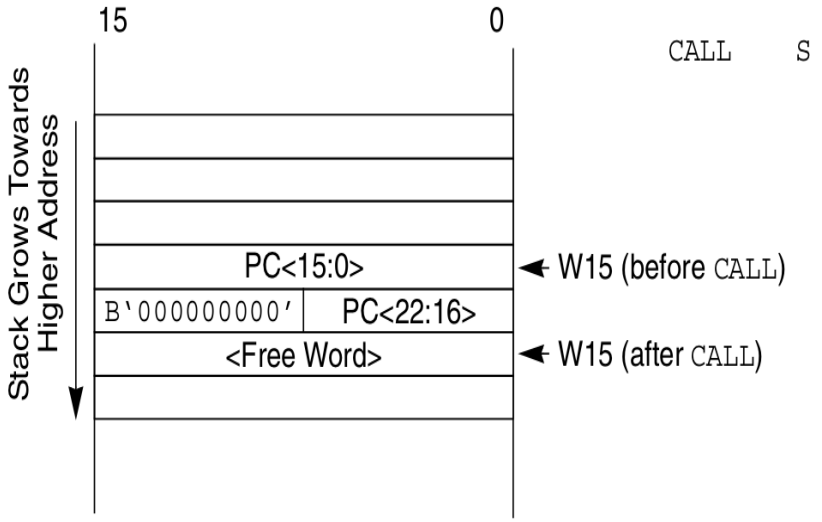
Familias de microcontroladores de 16 bits de Microchip

- Características generales
  - Periféricos, software y herramientas de desarrollo comunes a las 4 familias. Optimizados para C.
  - Memoria de programa desde 4KB a 256KB. Pila software. Interrupciones vectorizadas con prioridades.
  - Encapsulados de 14 a 100 pines, con pinout común.
  - Arquitectura Harvard modificada con bus de instrucción de 24 bits.
  - Ejecución de instrucciones en un sólo ciclo, incluidas multiplicación 16x16 y división 32/16 y 16/16
  - Respuesta a las interrupciones determinista (5 ciclos).
- Las 4 familias
  - PIC24F → bajo consumo
    - Bajo costo y bajo consumo (XLP). Alimentación a 3,3V
    - 16 MIPS y hasta 96KB de RAM
  - PIC24H → alto rendimiento
    - Alimentación a 3,3V
    - 40 MIPS, con canales de DMA y ADC de 10/12 bits de alto rendimiento
  - dsPIC30F → DSC versátil
    - Alimentación a 5V. Hasta 30MIPS. Motor DSP
    - Periféricos para control de potencia y de motores.
  - dsPIC33F → DSC alto rendimiento
    - Alimentación a 3,3V. Hasta 40 MIPS. Motor DSP
    - Periféricos para control de potencia y de motores.
    - ADC de alto rendimiento de 10/12 bits y hasta 32 canales

Breve vistazo a la arquitectura

- Instrucciones
  - Palabras de 24 bits
  - PC de 23 bits → máximo 4Mpalabras (12MB) de memoria de programa
  - Todas en 1 ciclo de instrucción ($2 \bullet T_{CY}$), excepto saltos, manejo de dobles y manejo de tablas
- 16 acumuladores → algunos con funciones especiales (distinto en dsPIC)
- Se puede mapear la memoria de datos en la de programa o al revés
- Pila Software
  - En memoria a partir de 0x0800
  - Crece en direcciones crecientes
  - Puntero de pila W15
  - Instrucciones PUSH/POP
  - Registro límite SPLIM
  - Protección → interrupción si se sale de la pila
  - Puntero marco de pila W14 → mecanismo para reservar memoria en la pila para pasar variables temporales (funciones) mediante las instrucciones LNK/ULNK



Comparación arquitecturas PIC24 y dsPIC

Figure 2-1: PIC24F CPU Core Block Diagram

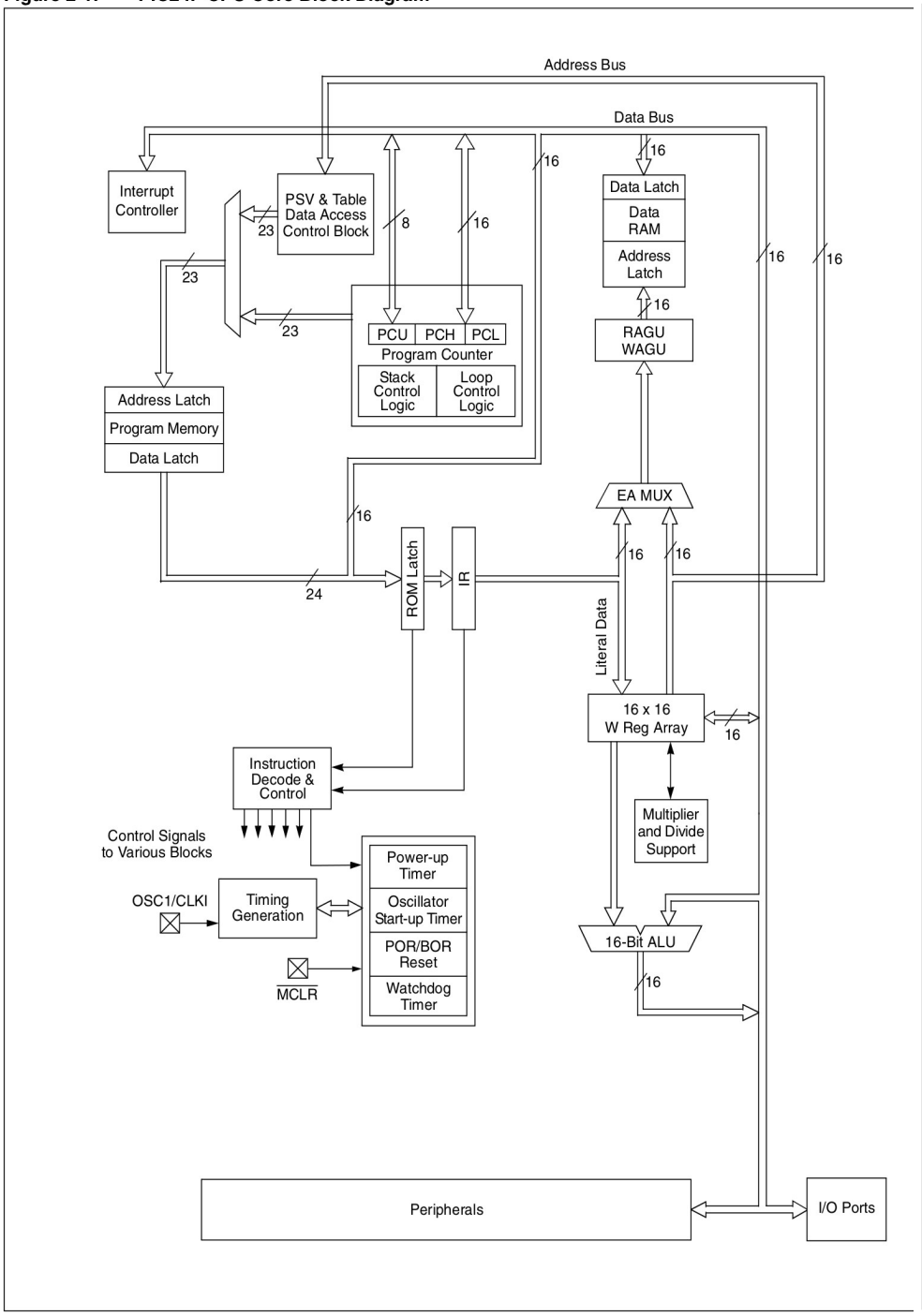
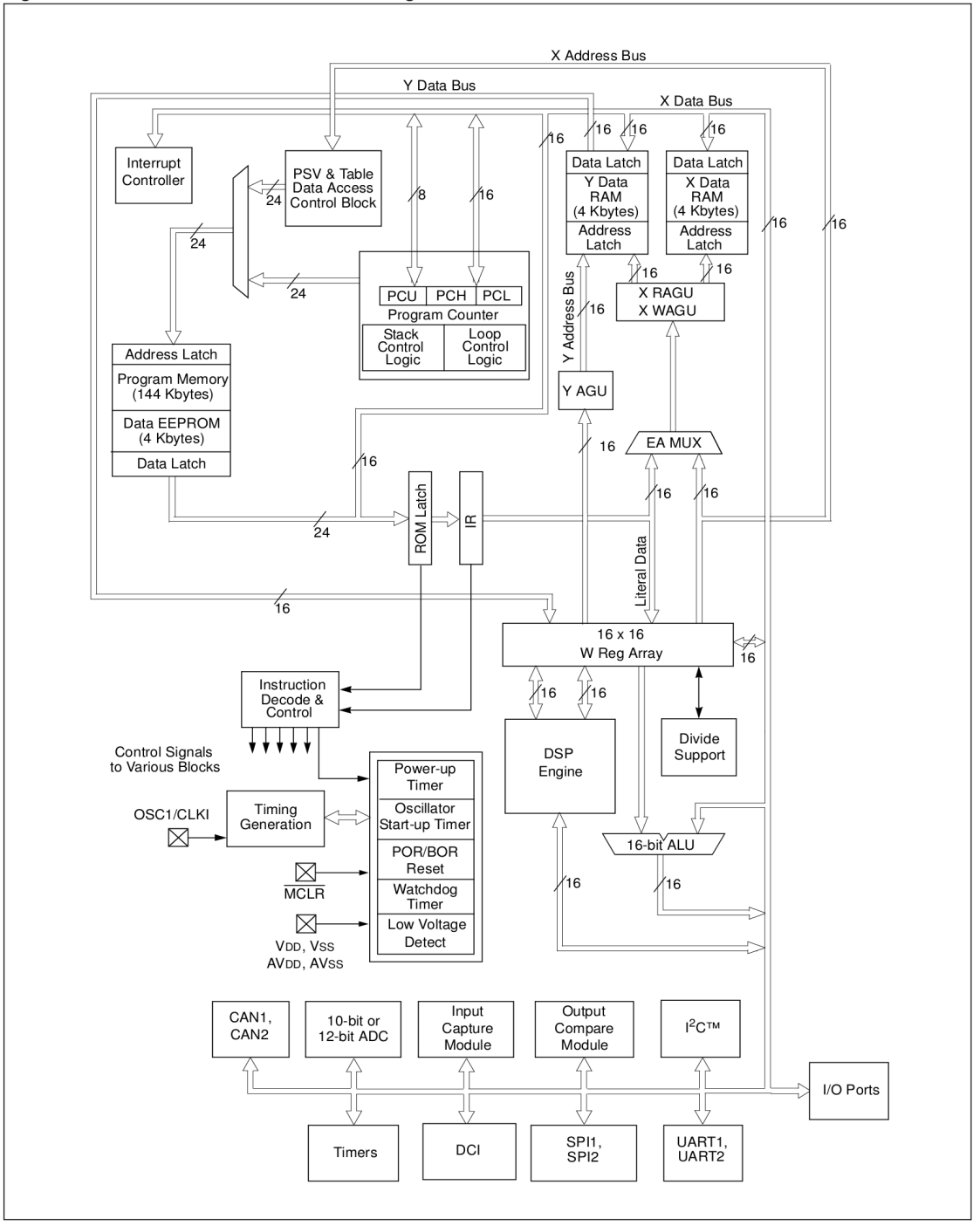
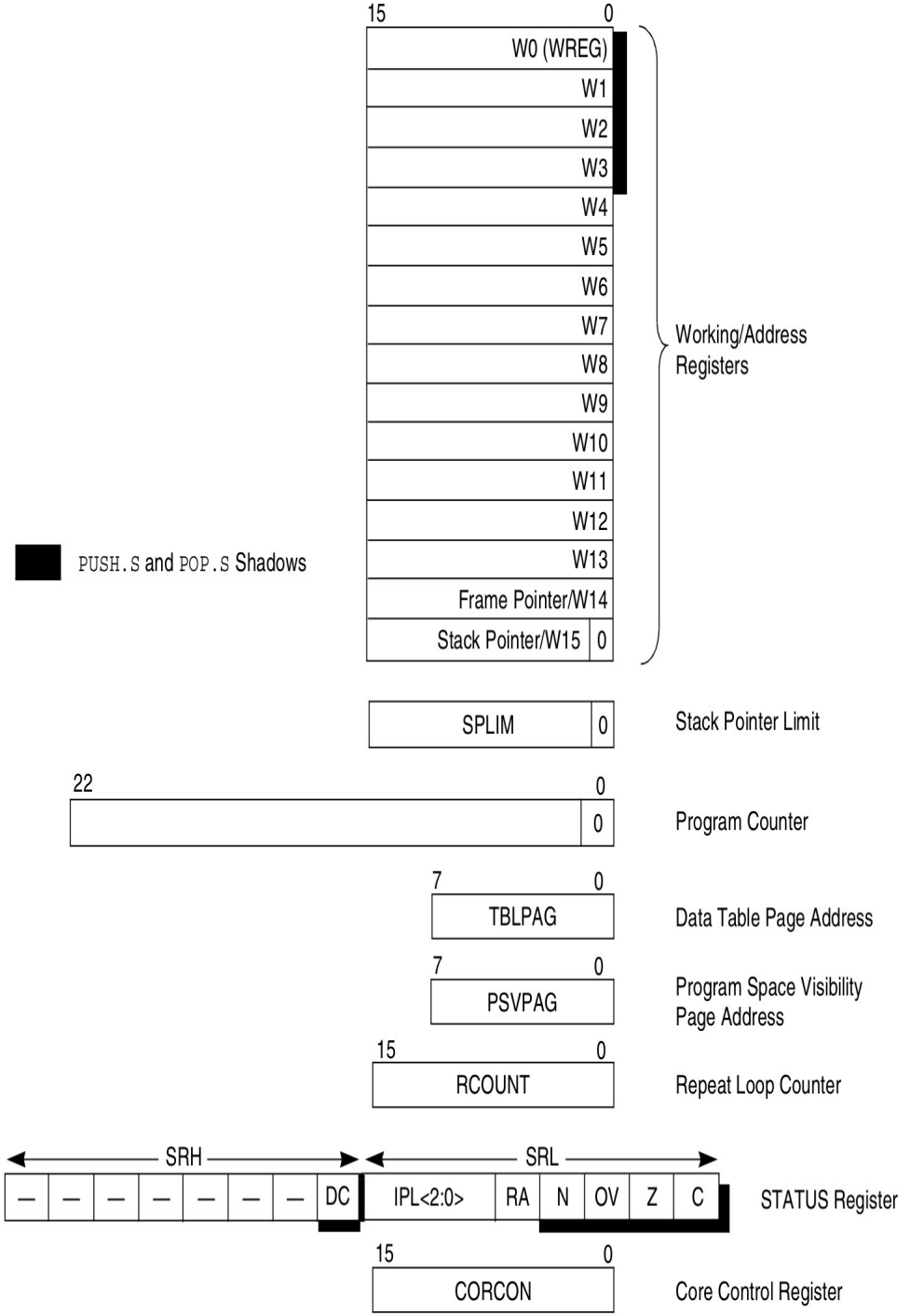


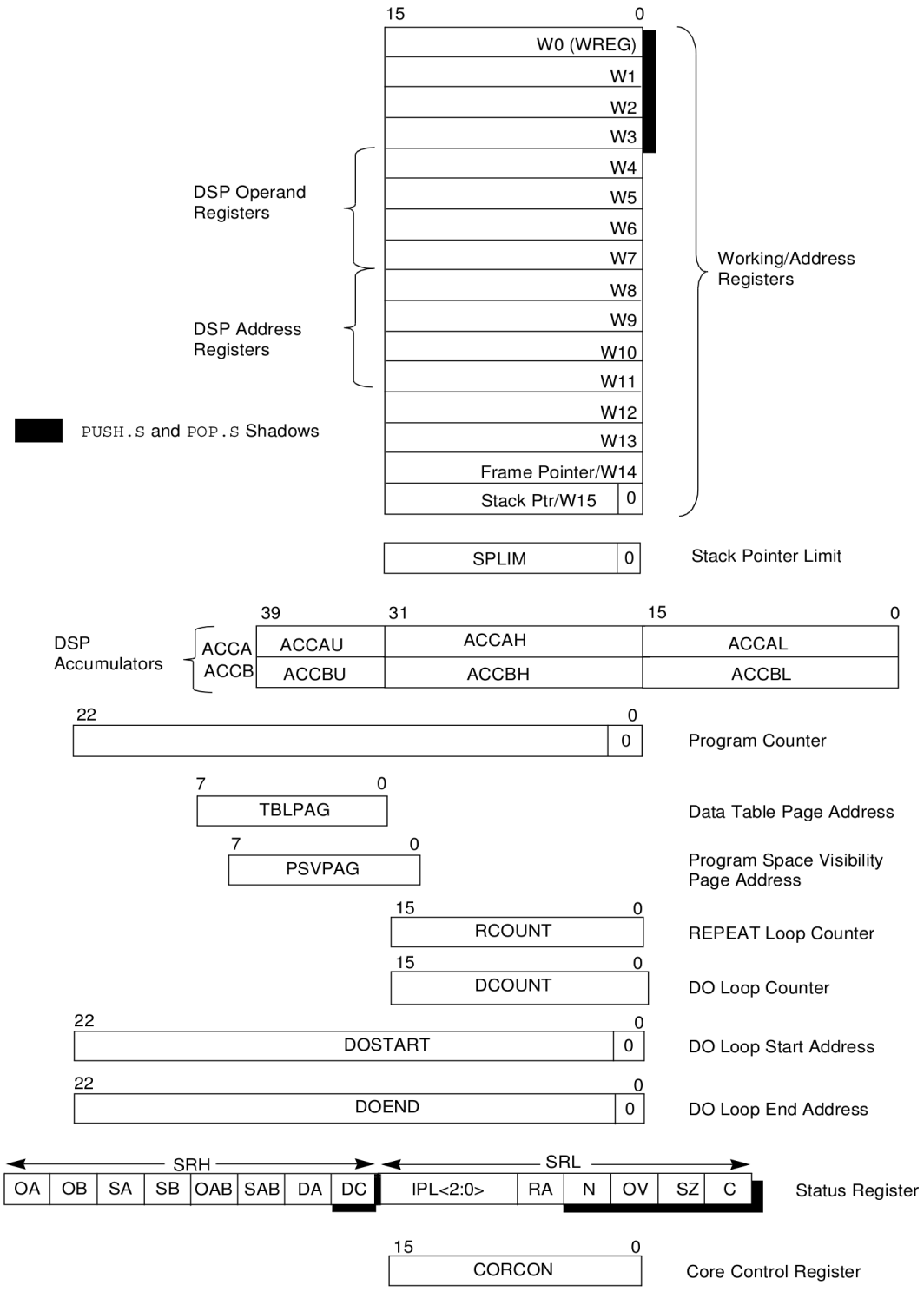
Figure 2-1: dsPIC30F CPU Core Block Diagram



PIC24F



dsPIC30F



Registros del núcleo, PIC24F

Register 2-1: SR: CPU STATUS Register

U-0	U-0	U-0	U-0	U-0	U-0	U -0	R/W-0
—	—	—	—	—	—	—	DC
bit 15							bit 8

R/W-0(2)	R/W-0(2)	R/W-0(2)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0>			RA	N	OV	Z	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
- 1 = A carry out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
- 0 = No carry out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(1)
- 111 = CPU interrupt priority level is 7 (15), user interrupts disabled
- 110 = CPU interrupt priority level is 6 (14)
- 101 = CPU interrupt priority level is 5 (13)
- 100 = CPU interrupt priority level is 4 (12)
- 011 = CPU interrupt priority level is 3 (11)
- 010 = CPU interrupt priority level is 2 (10)
- 001 = CPU interrupt priority level is 1 (9)
- 000 = CPU interrupt priority level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit
- 1 = REPEAT loop in progress
- 0 = REPEAT loop not in progress

bit 3 **N:** MCU ALU Negative bit
- 1 = Result was negative
- 0 = Result was non-negative (zero or positive)

bit 2 **OV:** MCU ALU Overflow bit
This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude which causes the sign bit to change state.
- 1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
- 0 = No overflow occurred

bit 1 **Z:** MCU ALU Zero bit
- 1 = Last operation resulted in zero
- 0 = Last operation did not result in zero

bit 0 **C:** MCU ALU Carry/$\overline{\text{Borrow}}$ bit
- 1 = A carry out from the Most Significant bit of the result occurred
- 0 = No carry out from the Most Significant bit of the result occurred

Note 1: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU interrupt priority level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

2: The IPL<2:0> Status bits are read-only when NSTDIS = 1 (INTCON1<15>).

Register 2-2: CORCON: Core Control Register

U-0	U-0	U-0	U-0	U-0	U-0	U -0	U -0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0	R/W-0	U-0	U-0
—	—	—	—	IPL3(1)	PSV	—	—
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit(1)
- 1 = CPU interrupt priority level is greater than 7
- 0 = CPU interrupt priority level is 7 or less

bit 2 **PSV:** Program Space Visibility in Data Space Enable bit
- 1 = Program space visible in data space
- 0 = Program space not visible in data space

bit 1-0 **Unimplemented:** Read as '0'

Note 1: User interrupts are disabled when IPL3 = 1.

Registros del núcleo dsPIC

Register 2-1: SR: CPU Status Register

Upper Byte:							
R-0	R-0	R/C-0	R/C-0	R-0	R/C-0	R -0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15							bit 8

Lower Byte: (SRL)							
R/W-0(2)	R/W-0(2)	R/W-0(2)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0>			RA	N	OV	Z	C
bit 7							bit 0

bit 15 **OA:** Accumulator A Overflow Status bit
1 = Accumulator A overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit
1 = Accumulator B overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

Note: This bit may be read or cleared (not set).

bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

Note: This bit may be read or cleared (not set).

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit
1 = Accumulators A or B have overflowed
0 = Neither Accumulators A or B have overflowed

bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit
1 = Accumulators A or B are saturated or have been saturated at some time in the past
0 = Neither Accumulator A or B are saturated

Note: This bit may be read or cleared (not set). Clearing this bit will clear SA and SB.

bit 9 **DA:** DO Loop Active bit
1 = DO loop in progress
0 = DO loop not in progress

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low order bit (for byte-sized data) or 8th low order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low order bit (for byte-sized data) or 8th low order bit (for word-sized data) of the result occurred

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(1)
111 = CPU Interrupt Priority Level is 7 (15). User interrupts disabled.
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

Note 1: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

2: The IPL<2:0> status bits are read only when NSTDIS = 1 (INTCON1<15>).

bit 4 **RA:** REPEAT Loop Active bit
1 = REPEAT loop in progress
0 = REPEAT loop not in progress

bit 3 **N:** MCU ALU Negative bit
1 = Result was negative
0 = Result was non-negative (zero or positive)

bit 2 **OV:** MCU ALU Overflow bit
This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude which causes the sign bit to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = No overflow occurred

bit 1 **Z:** MCU ALU Zero bit
1 = An operation which effects the Z bit has set it at some time in the past
0 = The most recent operation which effects the Z bit has cleared it (i.e., a non-zero result)

bit 0 **C:** MCU ALU Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Register 2-2: CORCON: Core Control Register

Upper Byte:							
U-0	U-0	U-0	R/W-0	R/W-0	R-0	R-0	R-0
—	—	—	US	EDT	DL<2:0>		
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3	PSV	RND	IF
bit 7							bit 0

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **US:** DSP Multiply Unsigned/Signed Control bit
1 = DSP engine multiplies are unsigned
0 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit
1 = Terminate executing DO loop at end of current loop iteration
0 = No effect

Note: This bit will always read as '0'.

bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits
111 = 7 DO loops active
•
•
001 = 1 DO loop active
000 = 0 DO loops active

bit 7 **SATA:** AccA Saturation Enable bit
1 = Accumulator A saturation enabled
0 = Accumulator A saturation disabled

bit 6 **SATB:** AccB Saturation Enable bit
1 = Accumulator B saturation enabled
0 = Accumulator B saturation disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit
1 = Data space write saturation enabled
0 = Data space write saturation disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit
1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3
1 = CPU interrupt priority level is greater than 7
0 = CPU interrupt priority level is 7 or less

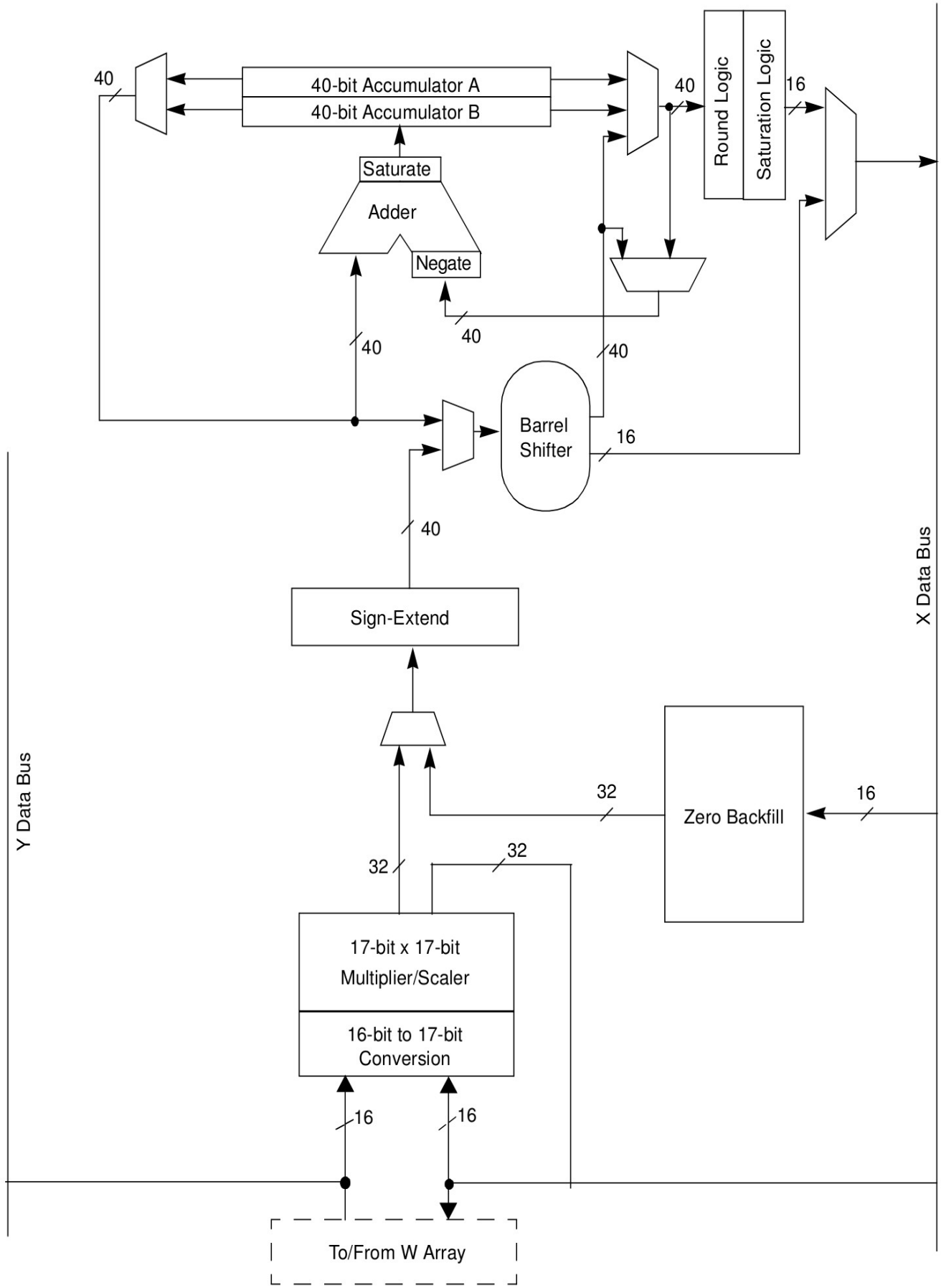
Note: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

bit 2 **PSV:** Program Space Visibility in Data Space Enable bit
1 = Program space visible in data space
0 = Program space not visible in data space

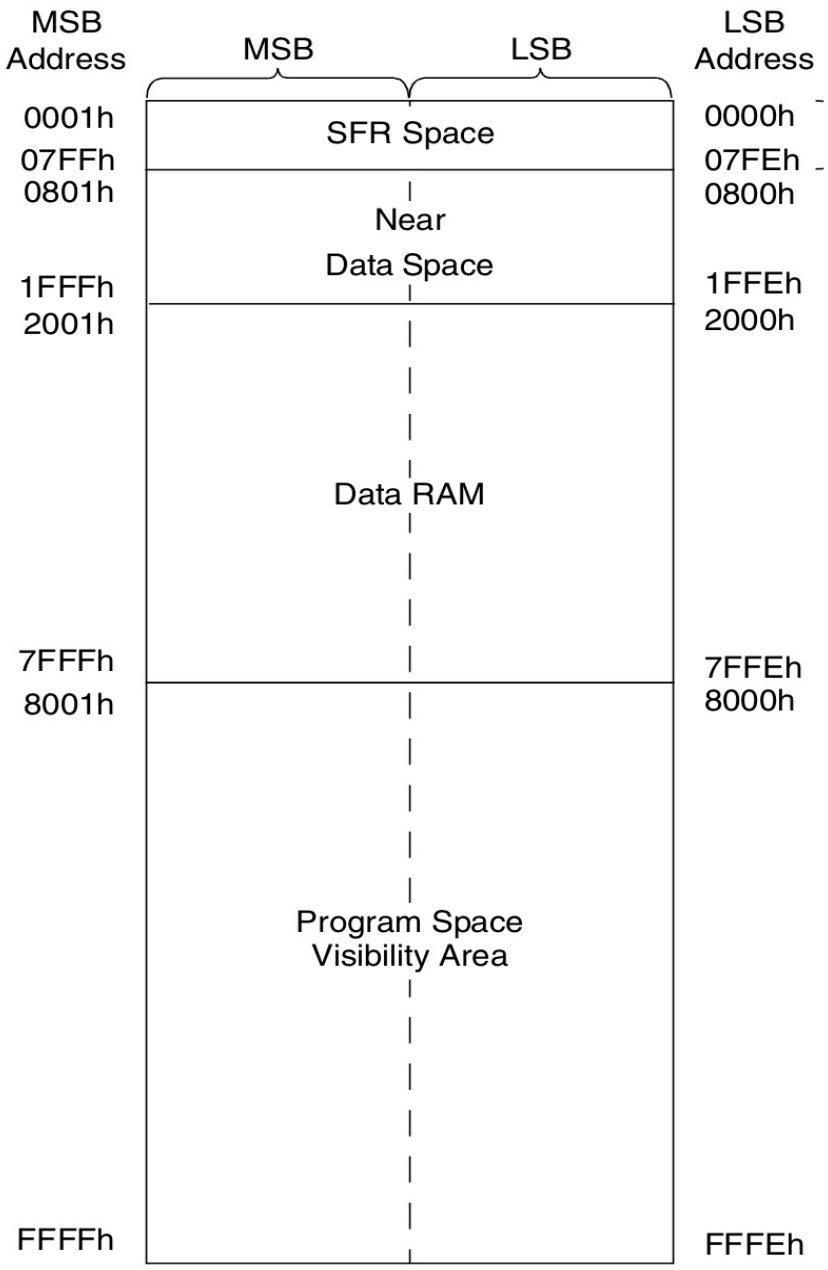
bit 1 **RND:** Rounding Mode Select bit
1 = Biased (conventional) rounding enabled
0 = Unbiased (convergent) rounding enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit
1 = Integer mode enabled for DSP multiply ops
0 = Fractional mode enabled for DSP multiply ops

Motor DSP

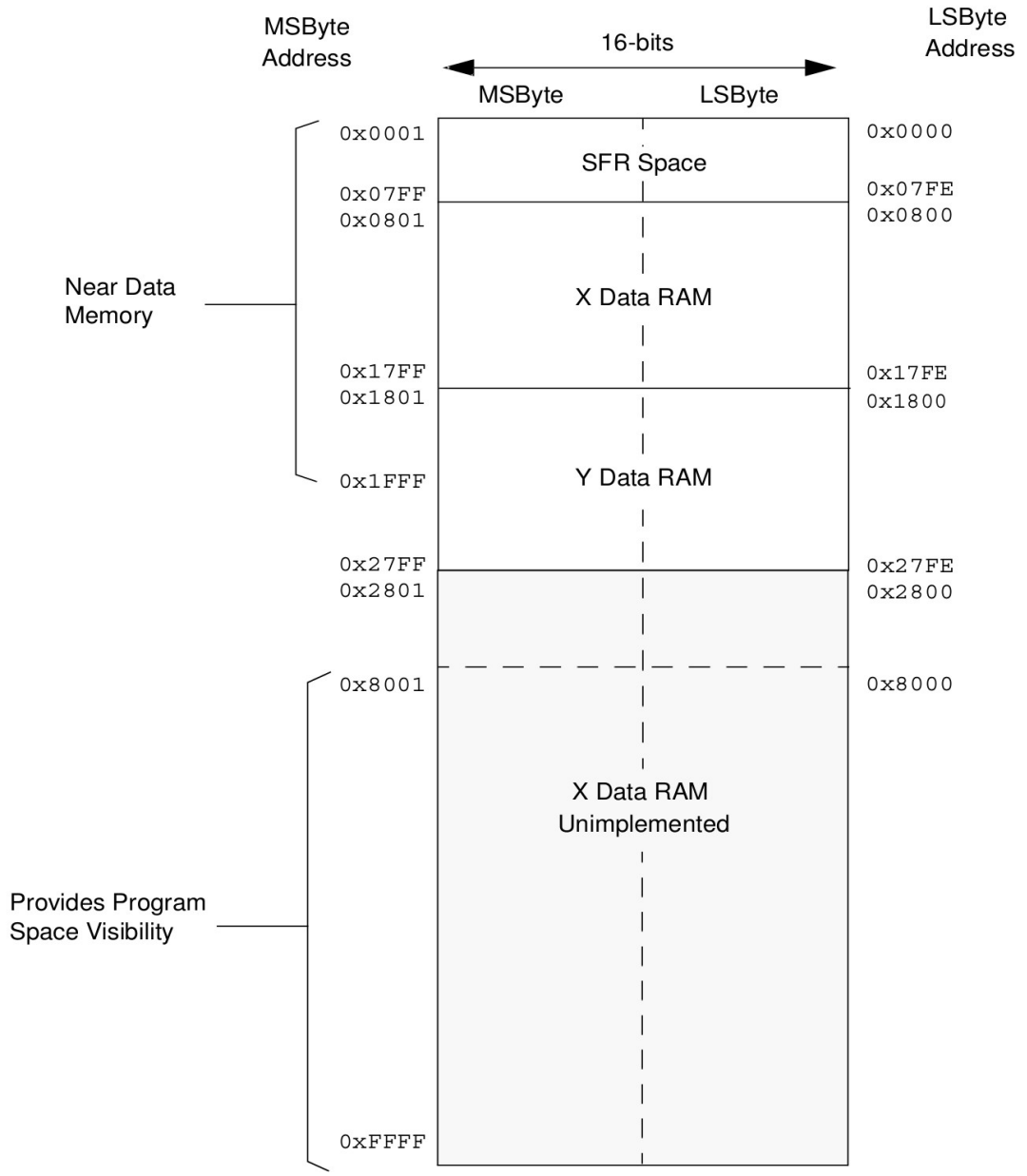

40
40-bit Accumulator A
40-bit Accumulator B
40
Round Logic
Saturation Logic
16
Saturate
Adder
Negate
40
40
40
40
Barrel
Shifter
16
40
Sign-Extend
Y Data Bus
X Data Bus
32
Zero Backfill
16
32
32
17-bit x 17-bit
Multiplier/Scaler
16-bit to 17-bit
Conversion
16
16
To/From W Array

Memoria de datos (PIC24)



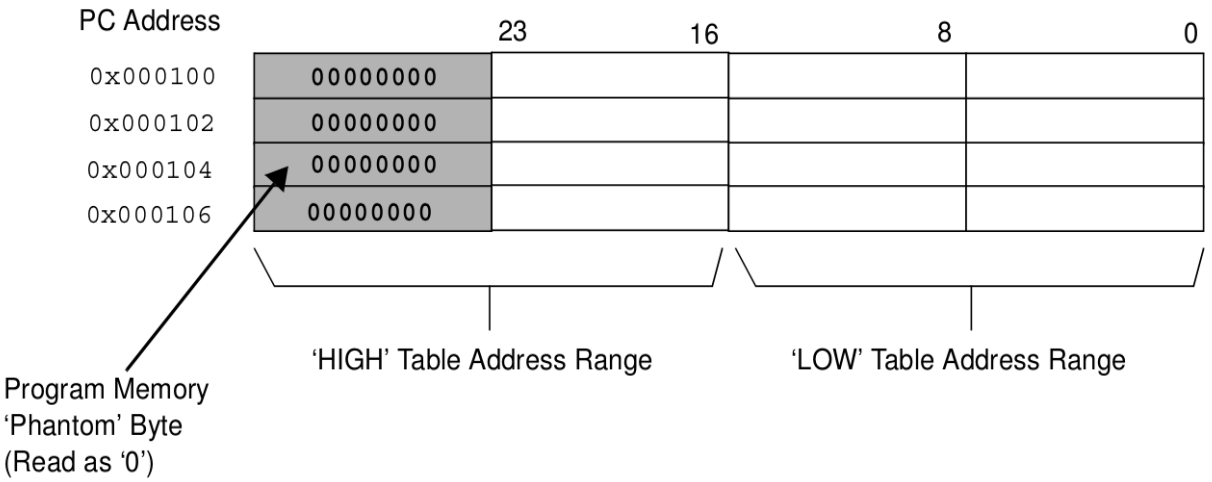
- Direcciones de 16 bits → 64K posiciones
- Posiciones de 16 bits → se puede
  - Direccionar como 32 K word
  - Direccionar como 64K bytes
    - MSB en direcciones pares
    - LSB en direcciones impares
  - Hay instrucciones de word y de byte
- Zonas
  - SFR → los registros
  - Espacio cercano (incluye SFR)
    - Dirección sólo de 13 bits
    - Accesible como registros (con todas las instrucciones de acceso a registros)
    - También accesible con direccionamiento indirecto
  - Resto del espacio RAM → sólo accesible mediante direccionamiento indirecto
  - Área de visibilidad del espacio de programa (PSV)
    - Permite mapear parte (seleccionable) de flash en RAM
    - Acceso (lectura) a los 16 bits bajos

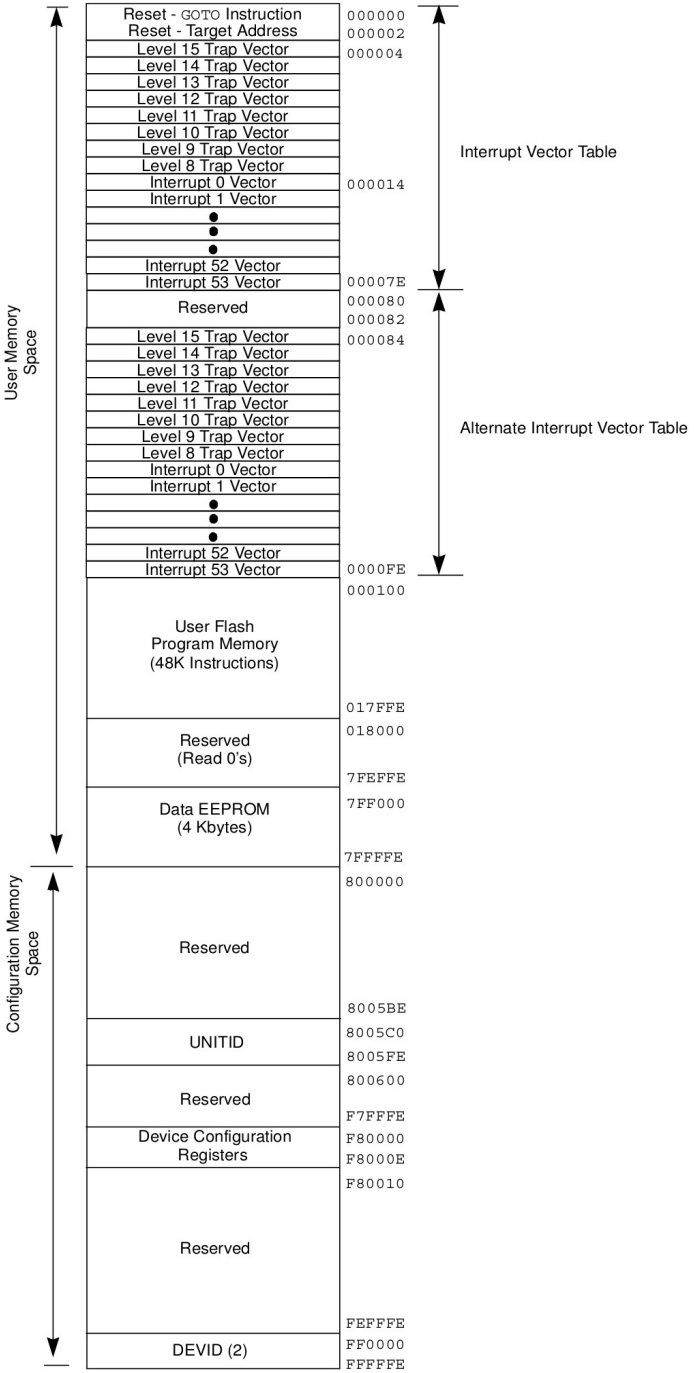
Memoria de datos (dsPIC)



- Igual que en PIC24 excepto para operaciones DSP
- Para DSP
  - Zonas X e Y con distintas funciones
    - Zona X → lectura y escritura
    - Zona Y → sólo lectura
  - Los límites de los espacios X e Y dependen de cada micro y además se pueden modificar
  - El multiplicador usa los espacios X e Y
    - Un dato de X y otro de Y
    - El resultado va siempre a X
    - Permite hacer la multiplicación en un sólo ciclo (con “prefetch” de los operandos)

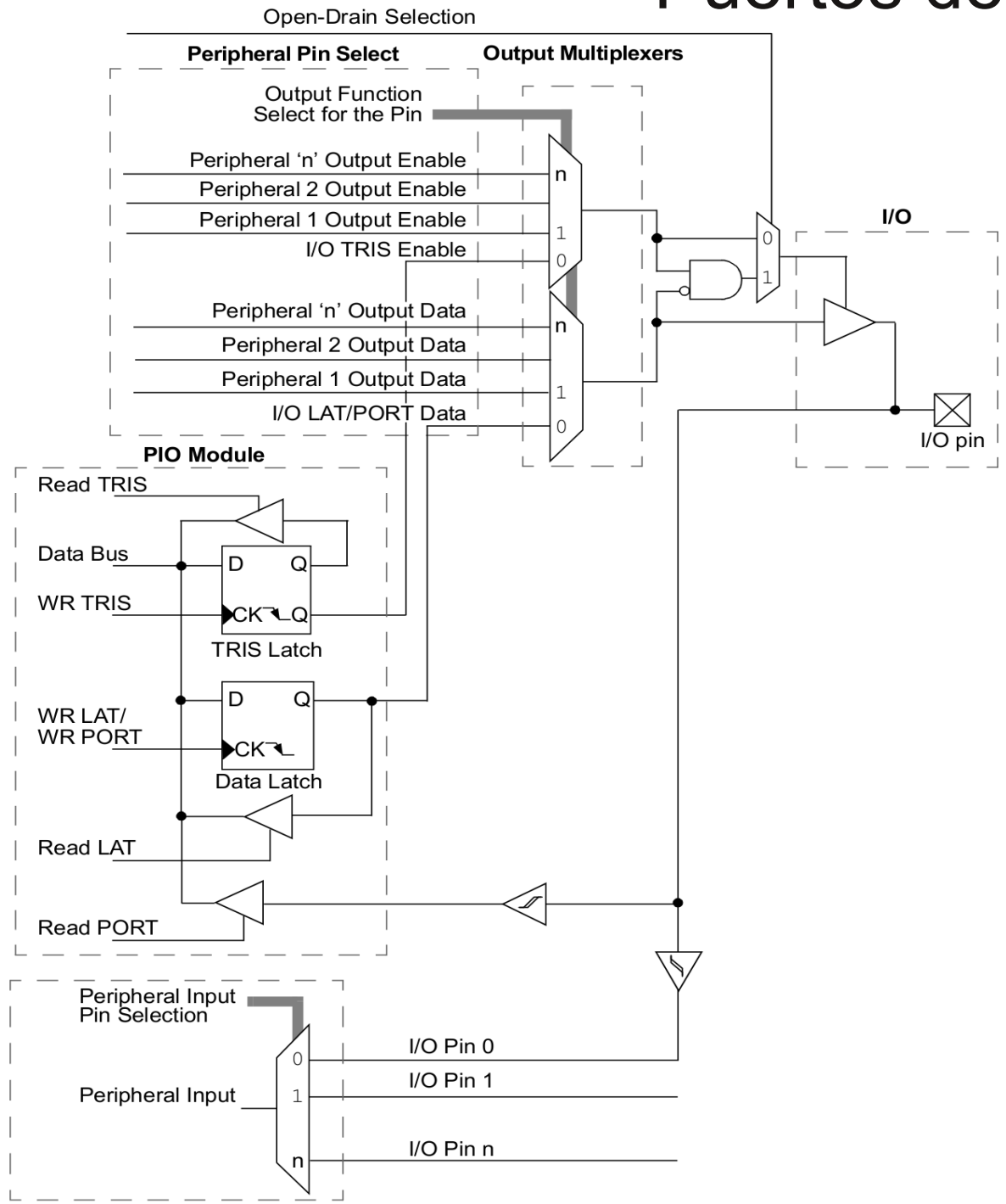
Memoria de programa





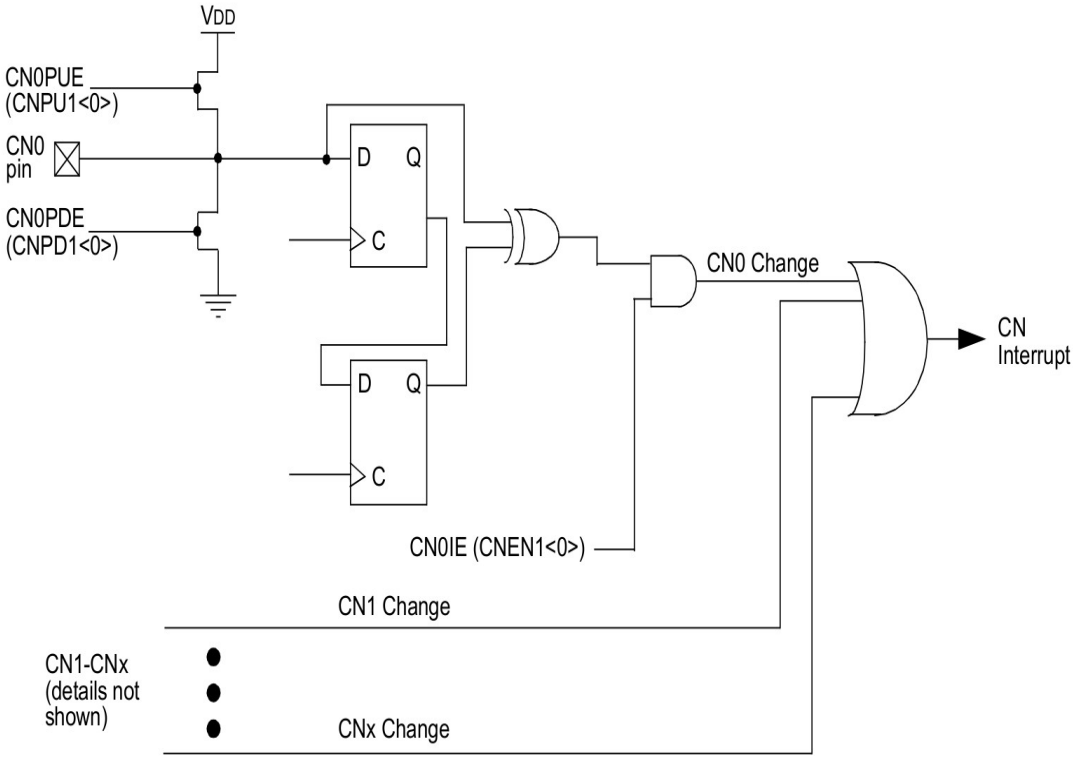
- Palabras de 24 bits
  - Se organizan como DWORD → MSB=0
  - En posiciones pares de memoria
- Accesible mediante
  - Directamente con PC
  - Mapeando un bloque (32KB) en RAM
  - Instrucciones de tabla
    - Acceso en lectura/escritura a los 24 bits
    - Instruciones TBLRDH, TBLWTH, TBLRDL, TBLWTL
    - Memoria dividida en páginas
      - 16 bits bajos de la dirección en la instrucción
      - 8 bits altos de la dirección: registro TBLPAG
    - La escritura de la memoria de programa con TBLWTH/TBLWTL no realiza realmente la escritura en FLASH, sino en unos latches La escritura real de la FLASH implica la escritura de un bloque de 32 direcciones mediante el uso de los registros NVMXXX
- Vectores de interrupción al principio de la memoria → cambian según el micro

Puertos de E/S



- Muy similares a los de la arquitectura mejorada de 8 bits, pero con todos los registros de 16 bits
- Registros asociados a cada puerto
  - TRISx → configuración E/S
  - PORTx → salida "física"
  - LATx → salida "lógica"
  - ODCx → configuración drenador abierto
    - Bit=1 → drenador abierto
    - No disponible en dsPIC30F
- Selección de pin de periférico (PPS)
  - Sólo en PIC24
  - Se pueden seleccionar pines (E o S)
  - Registros RPINRx → mapeo entradas
  - Registros RPORx → mapeo salidas
- Selección de pines A/D → ADPCFG

Interrupción en cambio de nivel



Muchos de los pines tiene la opción CN

Hasta 4 registros CNENx habilitan pin a pin la opción CN → bit=1 habilitado

Flag de interrupción único CNIF

(Des)habilitación global con CNIE

Pull-up programable:

- Disponible en todos los pines CN (entrada)
- Se habilita con registros CNPUx → pin a pin

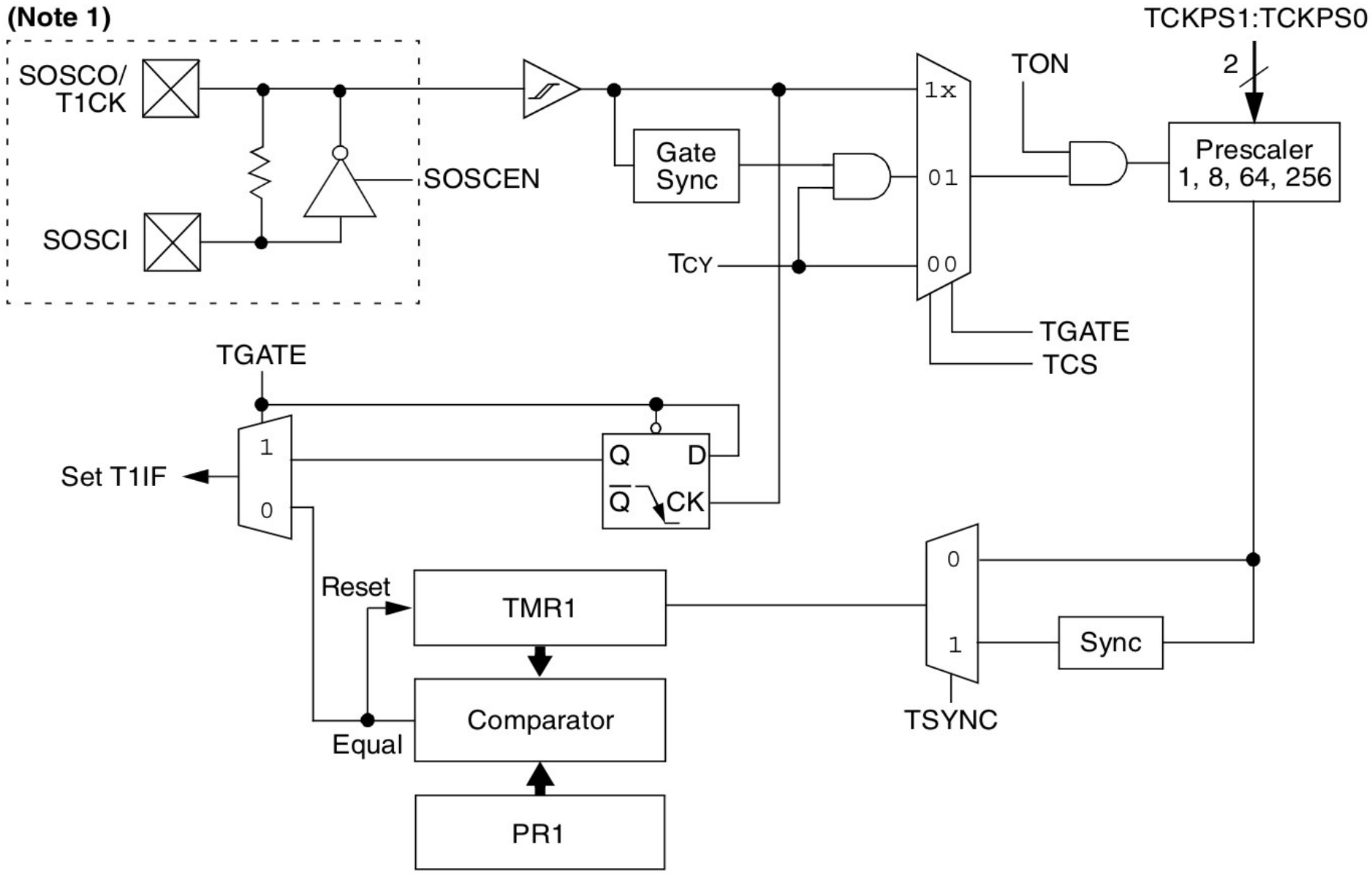
Pull-down programable

- Igual que pull-up, pero sólo en algunos micros
- Se habilita con registros CNPDx → pin a pin

Temporizadores

- Hasta 5 temporizadores de 16 bits
- Tres tipos distintos de temporizadores (A, B y C)
- Los tipos B y C pueden unirse para formar temporizadores de 32 bits
- Todos ellos disponen de
  - Registro TMRx → cuenta
  - Registro Prx → límite
  - Registro TxCON → control
  - Bits asociados en los registros de interrupciones
    - TxIE → habilitación de la interrupción (registros IECx)
    - TxIF → flag de interrupción (registros IFSx)
    - TxIP<2..0> → prioridad de la interrupción (registros IPCx)
  - Unos registros especiales TMRxHLD para poder leer el MSB de un registro de 32 bits
    - p.e si TMR3:TMR2 está configurado como registro de 32 bits, al leer TMR2 (el LSW), el contenido de TMR3 (el MSW) se copia al registro TMR3HLD para poder leerlo después.

Temporizador tipo A



Register 14-1: TxCON: Type A Time Base Control

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
—	TGATE	TCKPS<1:0>		—	TSYNC	TCS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timerx On bit
1 = Starts the timer
0 = Stops the timer

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Stop in Idle Mode bit
1 = Discontinue timer operation when device enters Idle mode
0 = Continue timer operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation enabled
0 = Gated time accumulation disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

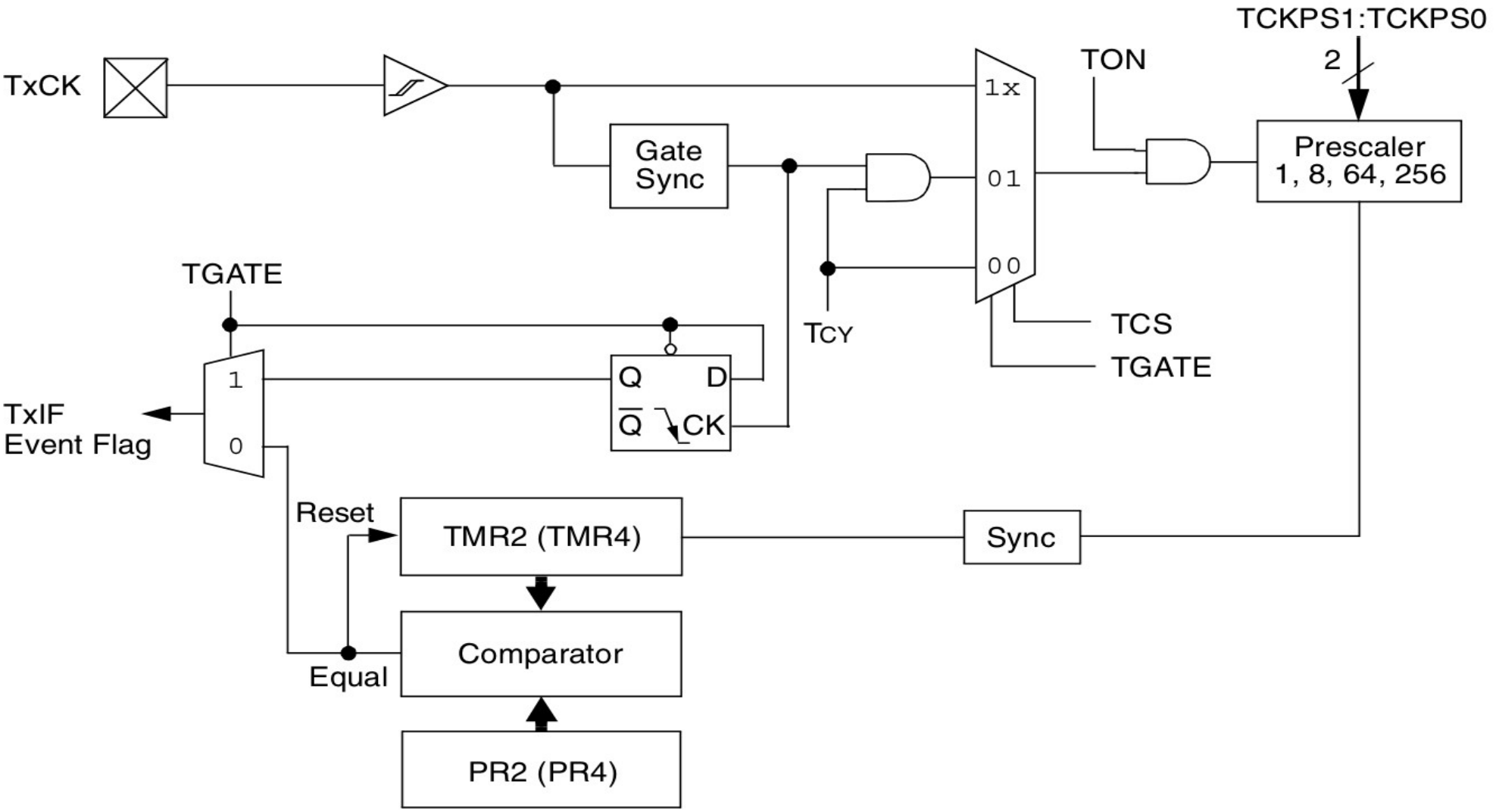
bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timerx External Clock Input Synchronization Select bit
When TCS = 1:
1 = Synchronize external clock input
0 = Do not synchronize external clock input
When TCS = 0:
This bit is ignored. Read as '0'. Timerx uses the internal clock when TCS = 0.

bit 1 **TCS:** Timerx Clock Source Select bit
1 = External clock from TxCK pin
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

Temporizador tipo B



Register 14-2: TxCON: Type B Time Base Control

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS<1:0>		T32	—	TCS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timerx On bit

When T32 = 1 (in 32-Bit Timer mode):
1 = Starts 32-bit TMRx:TMRy timer pair
0 = Stops 32-bit TMRx:TMRy timer pair

When T32 = 0 (in 16-Bit Timer mode):
1 = Starts 16-bit timer
0 = Stops 16-bit timer

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Stop in Idle Mode bit

1 = Discontinue timer operation when device enters Idle mode
0 = Continue timer operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit

When TCS = 1:
This bit is ignored.

When TCS = 0:
1 = Gated time accumulation enabled
0 = Gated time accumulation disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits

11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

bit 3 **T32:** 32-Bit Timerx Mode Select bit

1 = TMRx and TMRy form a 32-bit timer
0 = TMRx and TMRy form separate 16-bit timer

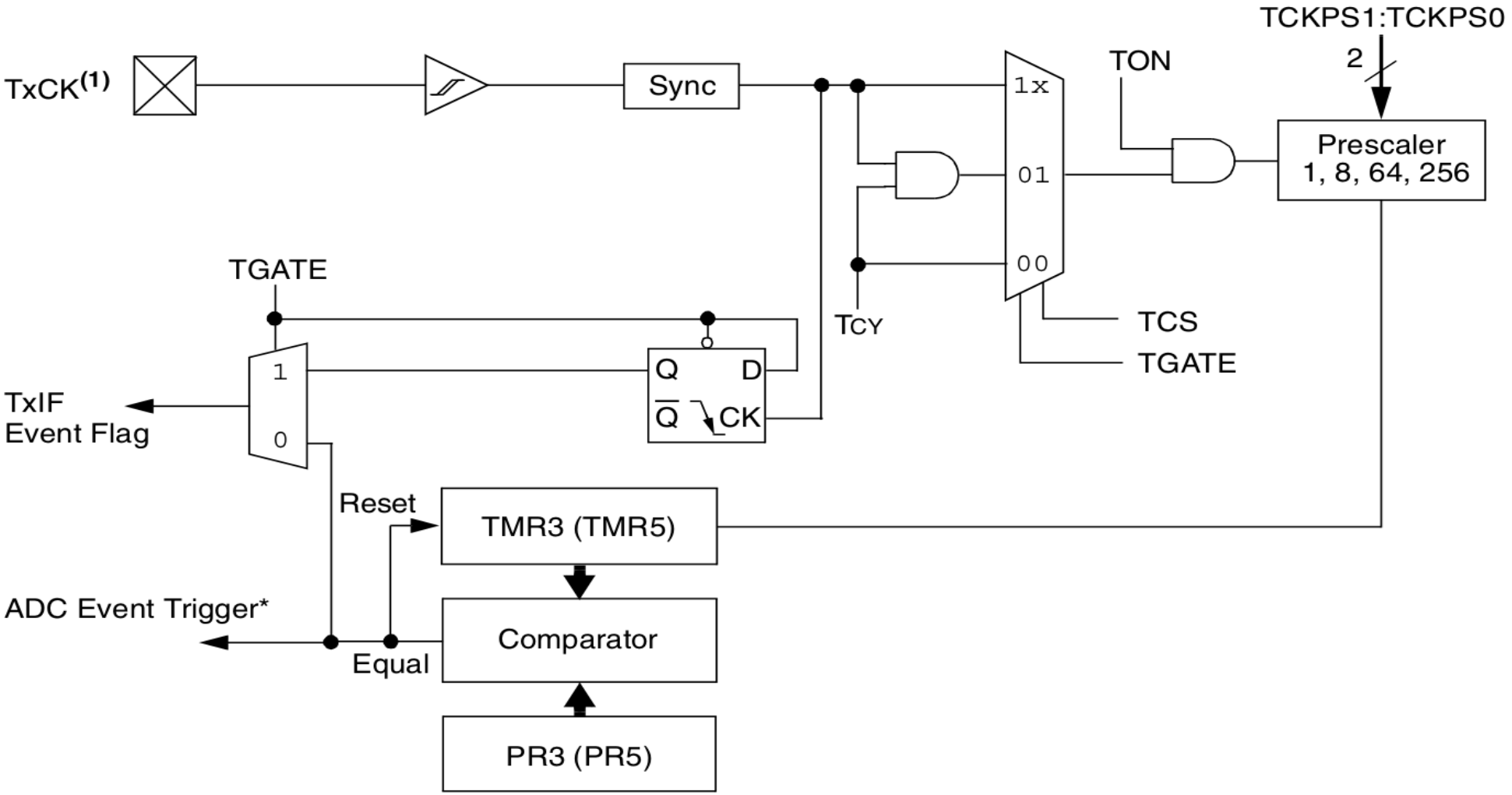
bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit

1 = External clock from TxCK pin
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

Temporizador tipo C



* The ADC Event Trigger is available only on Timer4/5.

Note 1: In certain variants of the PIC24F family, the TxCK pin may not be available. Refer to the device data sheet for the I/O pin details. In such cases, the timer must use the system clock (FOSC/2) as its input clock unless it is configured for 32-bit operation.

Register 14-3: TyCON: Type C Time Base Control

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(1)	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(1)	TCKPS<1:0>		—	—	TCS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timery On bit(1)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Stop in Idle Mode bit
1 = Discontinue timer operation when device enters Idle mode
0 = Continue timer operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation enabled
0 = Gated time accumulation disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

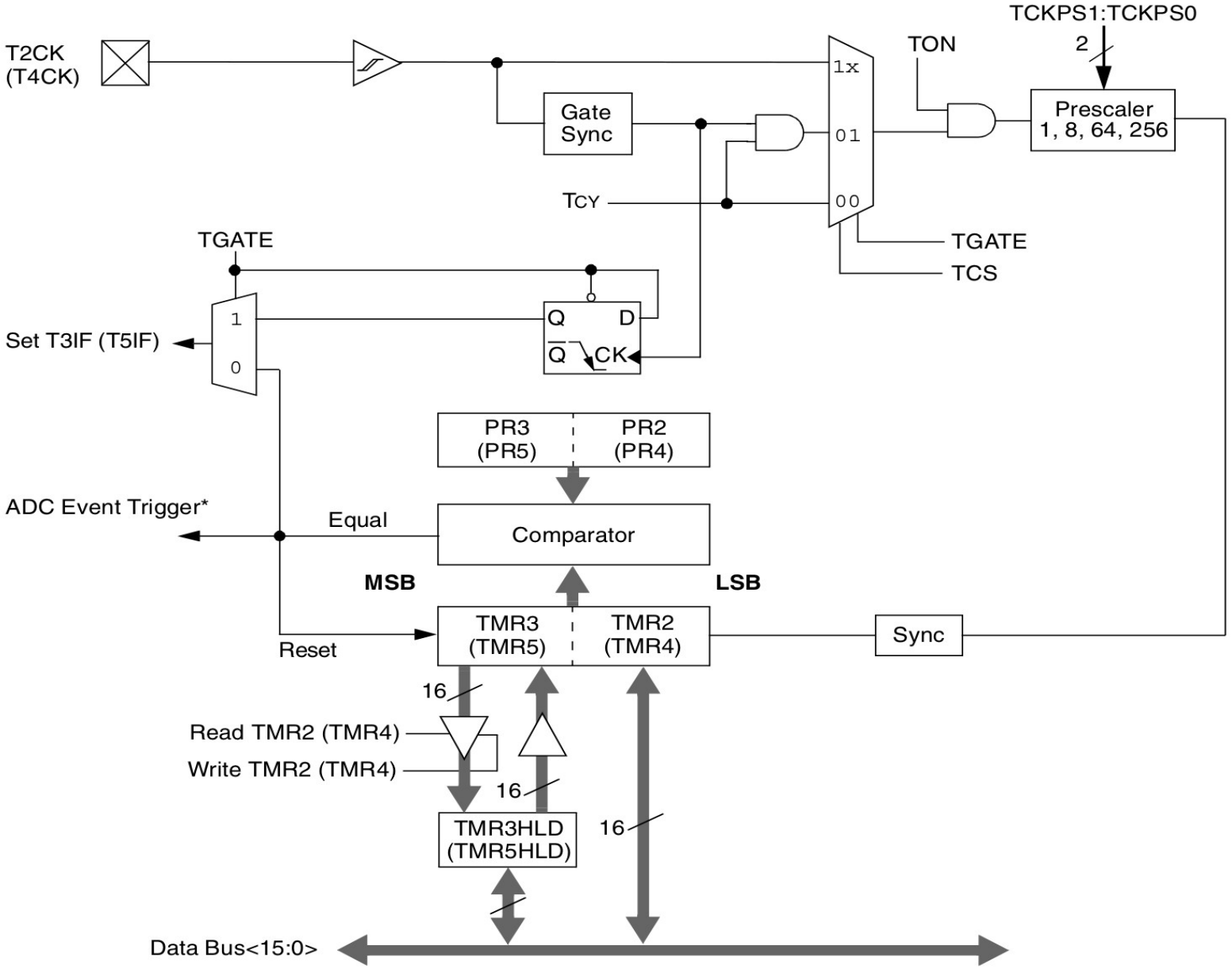
bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit
1 = External clock from TxCK pin
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through T2CON.

Temporizador de 32 bits (B+C)



* The ADC Event Trigger is available only on Timer4/5.

Note: The 32-bit Timer Configuration bit, T32, must be set for 32-bit timer/counter operation. All control bits are respective to the T2CON and T4CON registers.

Registros asociados con los temporizadores

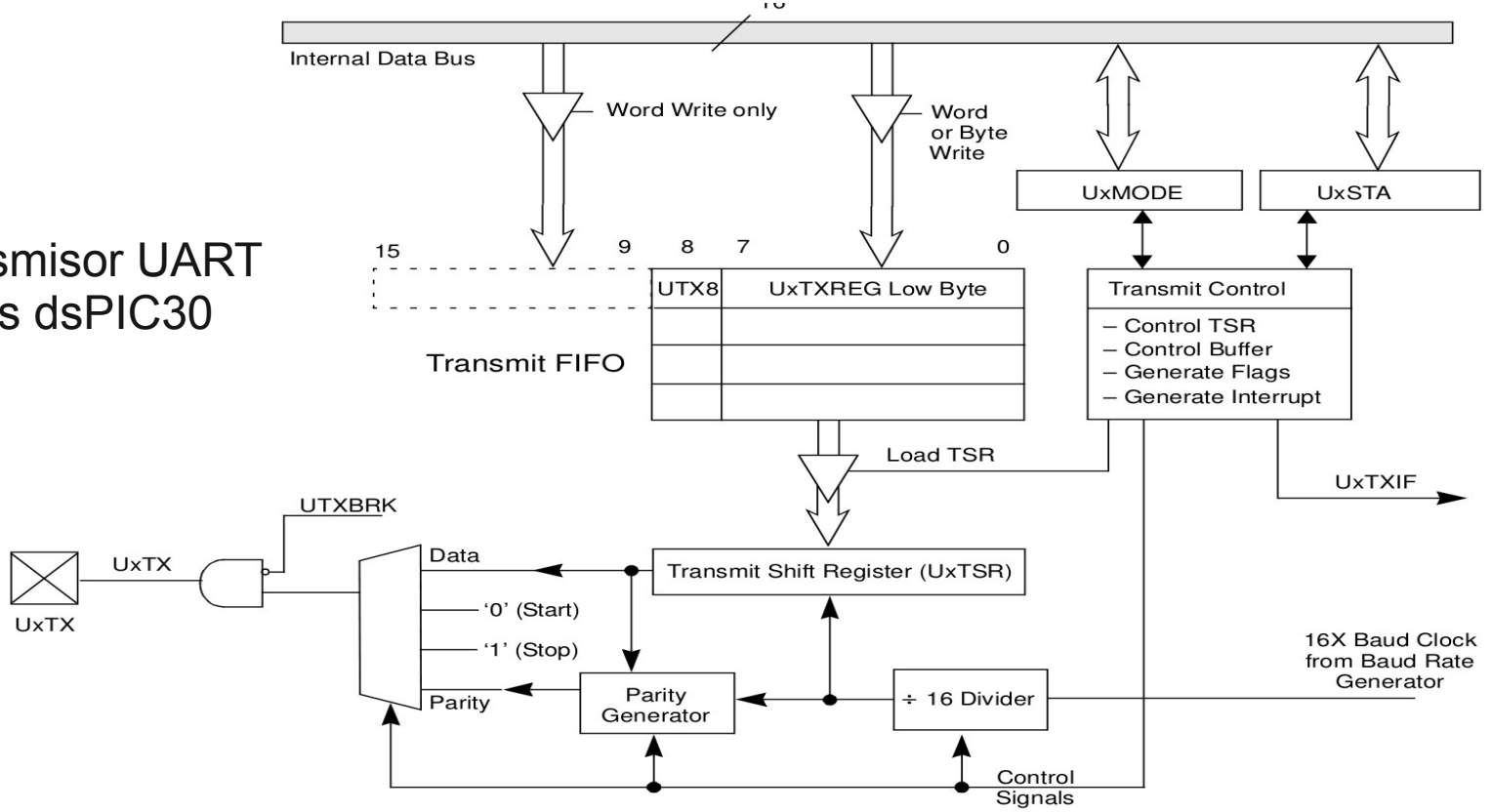
SFR Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	ADCMD	0000
TMR1	Timer1 Register																xxxx
PR1	Period Register 1																FFFF
T1CON	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—	0000
TMR2	Timer2 Register																xxxx
TMR3HLD	Timer3 Holding Register (for 32-bit timer operations only)																xxxx
TMR3	Timer3 Register																xxxx
PR2	Period Register 2																FFFF
PR3	Period Register 3																FFFF
T2CON	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T3CON	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR4	Timer4 Register																xxxx
TMR5HLD	Timer5 Holding Register (for 32-bit timer operations only)																xxxx
TMR5	Timer5 Register																xxxx
PR4	Period Register 4																FFFF
PR5	Period Register 5																FFFF
T4CON	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T5CON	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
IFS0	—	—	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPF1IF	T3IF	T2IF	OC2IF	IC2IF	—	T1IF	OC1IF	IC1IF	INT01F	0000
IFS1	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	—	—	—	—	INT1IF	CNIF	CMIF	M2C1IF	SI2C1IF	0000
IEC0	—	—	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPF1IE	T3IE	T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT01E	0000
IEC1	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	—	—	—	—	INT1IE	CNIE	CMIE	M2C1IE	SI2C1IE	0000
IPC0	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP0	4444
IPC1	—	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0	—	IC2IP2	IC2IP1	IC2IP0	—	—	—	—	4440
IPC2	—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	—	SPF1IP2	SPF1IP1	SPF1IP0	—	T3IP2	T3IP1	T3IP0	4444
IPC6	—	T4IP2	T4IP1	T4IP0	—	OC4IP2	OC4IP1	OC4IP0	—	OC3IP2	OC3IP1	OC3IP0	—	—	—	—	4440
IPC7	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2	T5IP1	T5IP0	4444

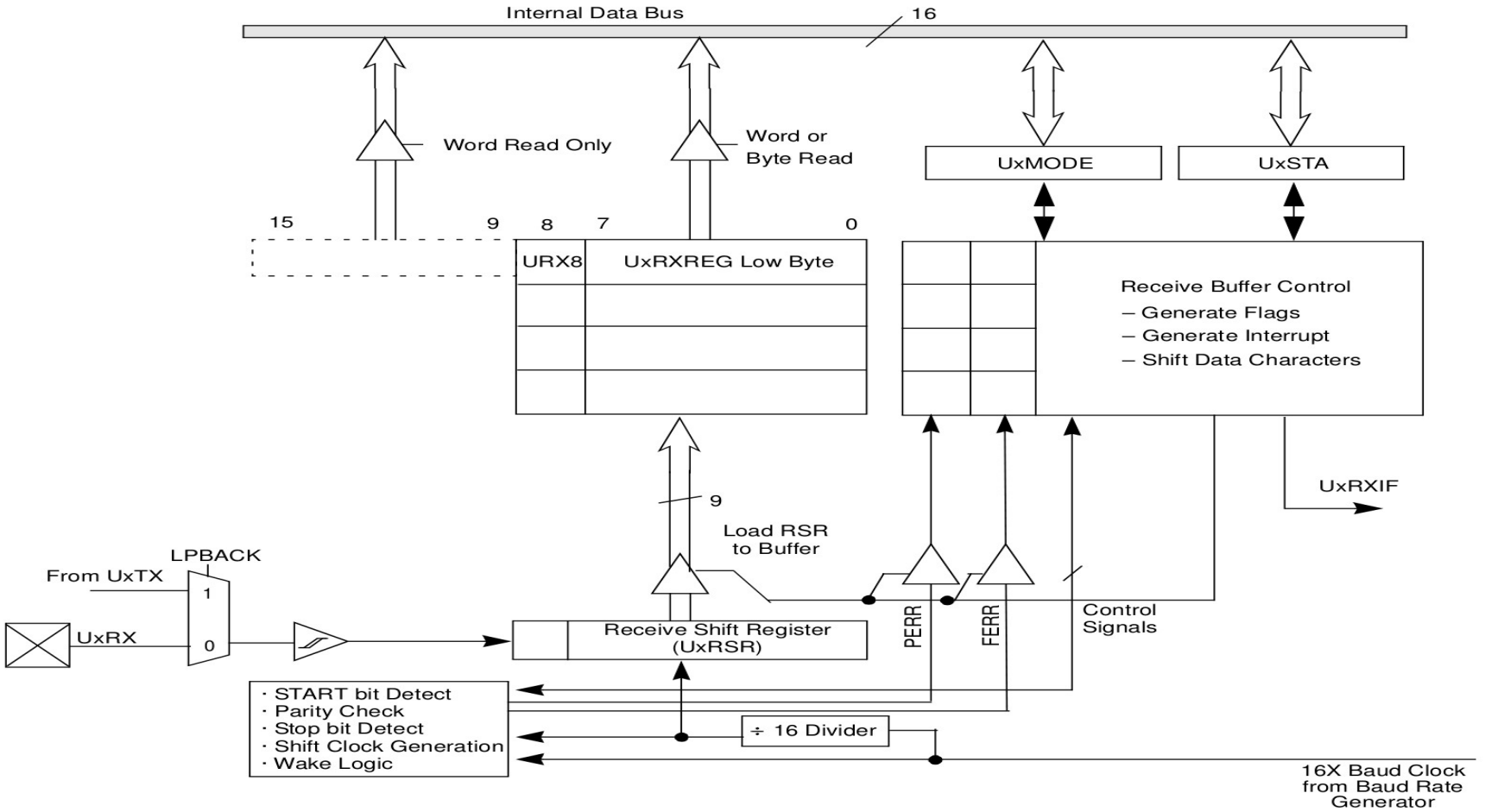
Note: Please refer to the specific device data sheet for memory map details.

UART

- En los dsPIC30 la UART es muy similar a la de los PIC de 8 bits, con algún cambio:
  - Los registros son de 16 bits, por lo que algunos bits de configuración cambian de sitio, p.e.: en los modos de TX/RX 9 bits el 9º bit se lee/escribe en el mismo registro RXREG/TXREG
  - Tiene un buffer de recepción y otro de transmisión ambos de 4 bytes → permite recibir o enviar 4 datos seguidos
- En los PIC24 y dsPIC33 la UART está ampliada
  - Puede usarse para transmisión serie RS232/RS485 igual que las anteriores
  - Puede soportar protocolos Lin1.2 (bus automoción) e IrDA (infrarrojos)

Transmisor UART
En los dsPIC30





19.12 Registers Associated with UART Module (dsPIC30)

Table 19-3: Registers Associated with UART1

SFR Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
U1MODE	UARTEN	—	USIDL	—	reserved	ALTIO	reserved	reserved	WAKE	LPBACK	ABAUD	—	—	PDSEL<1:0>		STSEL	0000 0000 0000 0000
U1STA	UTXISEL	—	—	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0000 0001 0001 0000
U1TXREG	—	—	—	—	—	—	—	UTX8	Transmit Register								0000 0000 0000 0000
U1RXREG	—	—	—	—	—	—	—	URX8	Receive Register								0000 0000 0000 0000
U1BRG	Baud Rate Generator Prescaler																0000 0000 0000 0000
IFS0	CNIF	MI2CIF	SI2CIF	NVMIF	ADIF	U1TXIF	U1RXIF	SPI1IF	T3IF	T2IF	OC2IF	IC2IF	T1IF	OC1IF	IC1IF	INT0	0000 0000 0000 0000
IEC0	CNIE	MI2CIE	SI2CIE	NVMIE	ADIE	U1TXIE	U1RXIE	SPI1IE	T3IE	T2IE	OC2IE	IC2IE	T1IE	OC1IE	IC1IE	INT0IE	0000 0000 0000 0000
IPC2	—	ADIP<2:0>			—	U1TXIP<2:0>			—	U1RXIP<2:0>			—	SPI1IP<2:0>			0100 0100 0100 0100

Note: The registers associated with UART1 are shown for reference. See the device data sheet for the registers associated with other UART modules.

Register 19-1: UxMODE: UARTx Mode Register

Upper Byte:							
R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	U-0	U-0
UARTEN	—	USIDL	—	reserved	ALTIO	reserved	reserved
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	—	—	PDSEL<1:0>		STSEL
bit 7							bit 0

bit 15 **UARTEN:** UART Enable bit
1 = UART is enabled. UART pins are controlled by UART as defined by UEN<1:0> and UTXEN control bits.
0 = UART is disabled. UART pins are controlled by corresponding PORT, LAT, and TRIS bits.

bit 14 **Unimplemented:** Read as '0'

bit 13 **USIDL:** Stop in Idle Mode bit
1 = Discontinue operation when device enters Idle mode
0 = Continue operation in Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **Reserved:** Write '0' to this location

bit 10 **ALTIO:** UART Alternate I/O Selection bit
1 = UART communicates using UxATX and UxARX I/O pins
0 = UART communicates using UxTX and UxRX I/O pins

Note: The alternate UART I/O pins are not available on all devices. See device data sheet for details.

bit 9-8 **Reserved:** Write '0' to these locations

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
1 = Wake-up enabled
0 = Wake-up disabled

bit 6 **LPBACK:** UART Loopback Mode Select bit
1 = Enable Loopback mode
0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto Baud Enable bit
1 = Input to Capture module from UxRX pin
0 = Input to Capture module from ICx pin

bit 4-3 **Unimplemented:** Read as '0'

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

Register 19-2: UxSTA: UARTx Status and Control Register

Upper Byte:

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R-0	R-1
UTXISEL	—	—	—	UTXBRK	UTXEN	UTXBF	TRMT
bit 15							bit 8

Lower Byte:

R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

bit 15 **UTXISEL:** Transmission Interrupt Mode Selection bit
1 = Interrupt when a character is transferred to the Transmit Shift register and as result, the transmit buffer becomes empty
0 = Interrupt when a character is transferred to the Transmit Shift register (this implies that there is at least one character open in the transmit buffer)

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **UTXBRK:** Transmit Break bit
1 = UxTX pin is driven low, regardless of transmitter state
0 = UxTX pin operates normally

bit 10 **UTXEN:** Transmit Enable bit
1 = UART transmitter enabled, UxTX pin controlled by UART (if UARTEN = 1)
0 = UART transmitter disabled, any pending transmission is aborted and buffer is reset. UxTX pin controlled by PORT.

bit 9 **UTXBF:** Transmit Buffer Full Status bit (Read Only)
1 = Transmit buffer is full
0 = Transmit buffer is not full, at least one more data word can be written

bit 8 **TRMT:** Transmit Shift Register is Empty bit (Read Only)
1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer

bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Interrupt flag bit is set when Receive Buffer is full (i.e., has 4 data characters)
10 = Interrupt flag bit is set when Receive Buffer is 3/4 full (i.e., has 3 data characters)
0x = Interrupt flag bit is set when a character is received

bit 5 **ADDEN:** Address Character Detect (bit 8 of received data = 1)
1 = Address Detect mode enabled. If 9-bit mode is not selected, this control bit has no effect.
0 = Address Detect mode disabled

bit 4 **RIDLE:** Receiver Idle bit (Read Only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (Read Only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (Read Only)
1 = Framing Error has been detected for the current character
0 = Framing Error has not been detected

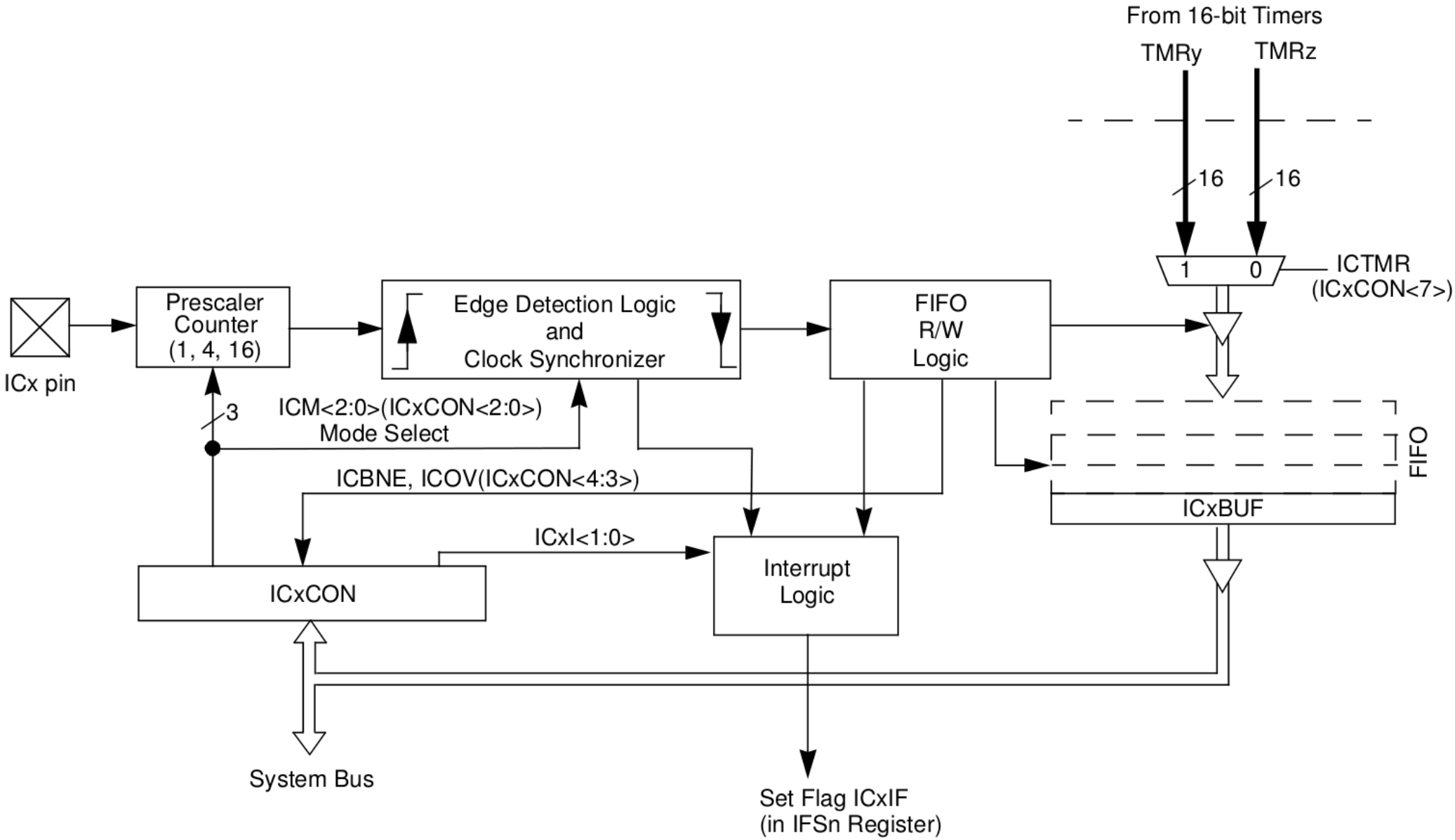
bit 1 **OERR:** Receive Buffer Overrun Error Status bit (Read/Clear Only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** Receive Buffer Data Available bit (Read Only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

Módulo Captura/Comparación/PWM

- El funcionamiento es muy similar al del módulo en los PIC de 8 bits
- Cambian bits de configuración que cambian de registro o de nombre
- Cambia el tamaño de los registros
- En modo captura, en vez de haber un único registro para capturar el valor del TMR, hay un buffer FIFO de 4 niveles
- En modo comparación
  - Cada módulo se puede asociar al TMR2 o TMR3
  - Cambian los modos de comparación (más modos y más flexible)
  - Dos registros distintos (OCxR y OCxRS), para hacer comparaciones dobles
- En modo PWM
  - La resolución es de 16 bits (porque el registro límite del TMR es de 16 bits)
  - PWM Period = [(PRy) + 1] • T_{CY} • (TMRy Prescale Value) → Tcy=2•T_{CLK}
- Dos “módulos” distintos para PWM
  - El PWM “normal” es un modo del módulo de Comparación
  - Un módulo aparte (sólo en algunos micros) denominado MCPWM (Motor Control PWM) con un funcionamiento totalmente distinto del anterior para generar señales PWM sincronizadas → control de motores trifásicos, etc.

Módulo de captura



Note: An ‘x’ in a signal, register or bit name denotes the number of the capture channel.

Register 13-1: ICxCON: Input Capture x Control Register

Upper Byte:							
U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		
bit 7							bit 0

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Module Stop in Idle Control bit
1 = Input capture module will halt in CPU Idle mode
0 = Input capture module will continue to operate in CPU Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **ICTMR:** Input Capture Timer Select bits
1 = TMR2 contents are captured on capture event
0 = TMR3 contents are captured on capture event

Note: Timer selections may vary. Refer to the device data sheet for details.

bit 6-5 **ICI<1:0>:** Select Number of Captures per Interrupt bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag (Read Only) bit
1 = Input capture overflow occurred
0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Empty Status (Read Only) bit
1 = Input capture buffer is not empty, at least one more capture value can be read
0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
111 = Input Capture functions as interrupt pin only, when device is in Sleep or Idle mode
(Rising edge detect only, all other control bits are not applicable.)
110 = Unused (module disabled)
101 = Capture mode, every 16th rising edge
100 = Capture mode, every 4th rising edge
011 = Capture mode, every rising edge
010 = Capture mode, every falling edge
001 = Capture mode, every edge (rising and falling)
(ICI<1:0> does not control interrupt generation for this mode.)
000 = Input capture module turned off

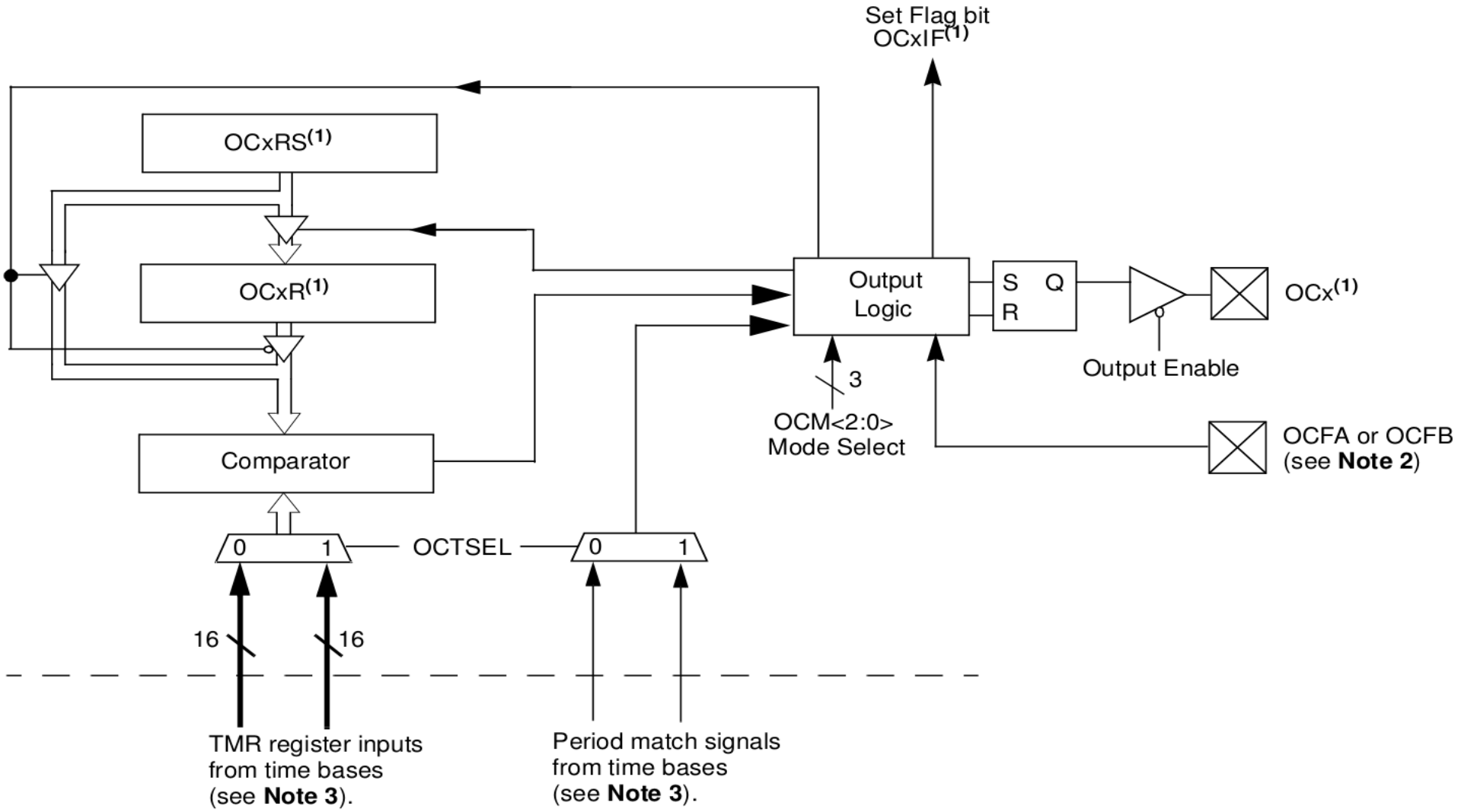
Table 13-1: Example Memory Map for Input Capture Modules

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
IFS0	0084	CNIF	MI2CIF	SI2CIF	NVMIF	ADIF	U1TXIF	U1RXIF	SPI1IF	T3IF	T2IF	OC2IF	IC2IF	T1IF	OC1IF	IC1IF	INT0F	0000 0000 0000 0000
IFS1	0086	IC6IF	IC5IF	IC4IF	IC3IF	C1IF	SPI2IF	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	IC8IF	IC7IF	INT1IF	0000 0000 0000 0000
IEC0	008C	CNIE	MI2CIE	SI2CIE	IR12	ADIE	U1TXIE	U1RXIE	SPI1IE	T3IE	T2IE	OC2IE	IC2IE	T1IE	OC1IE	IC1IE	INT0IE	0000 0000 0000 0000
IEC1	008E	IC6IE	EI30	IC4IE	IC3IE	C1IE	SPI2IE	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	IC8IE	IC7IE	INT1IE	0000 0000 0000 0000
IPC0	0094	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			0100 0100 0100 0100
IPC1	0096	—	T31P<2:0>			—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			0100 0100 0100 0100
IPC4	009C	—	OC3IP<2:0>			—	IC8IP<2:0>			—	IC7IP<2:0>			—	INT1IP<2:0>			0100 0100 0100 0100
IPC7	00A2	—	IC6IP<2:0>			—	IC5IP<2:0>			—	IC4IP<2:0>			—	IC3IP<2:0>			0100 0100 0100 0100
IC1BUF	0140	Input 1 Capture Register																uuuu uuuu uuuu uuuu
IC1CON	0142	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000 0000 0000 0000
IC2BUF	0144	Input 2 Capture Register																uuuu uuuu uuuu uuuu
IC2CON	0146	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000 0000 0000 0000
IC3BUF	0148	Input 3 Capture Register																uuuu uuuu uuuu uuuu
IC3CON	014A	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000 0000 0000 0000
IC4BUF	014C	Input 4 Capture Register																uuuu uuuu uuuu uuuu
IC4CON	014E	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000 0000 0000 0000
IC5BUF	0150	Input 5 Capture Register																uuuu uuuu uuuu uuuu
IC5CON	0152	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000 0000 0000 0000
IC6BUF	0154	Input 6 Capture Register																uuuu uuuu uuuu uuuu
IC6CON	0156	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000 0000 0000 0000
IC7BUF	0158	Input 7 Capture Register																uuuu uuuu uuuu uuuu
IC7CON	015A	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000 0000 0000 0000
IC8BUF	015C	Input 8 Capture Register																uuuu uuuu uuuu uuuu
IC8CON	015E	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000 0000 0000 0000

Legend: u = uninitialized

Note: Refer to the device data sheet for specific memory map details.

Módulo de comparación



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels 1 through 8.

2: OCFA pin controls OC1-OC4 channels. OCFB pin controls OC5-OC8 channels.

3: Each output compare channel can use one of two selectable time bases. Refer to the device data sheet for the time bases associated with the module.

Register 14-1: OCxCON: Output Compare x Control Register

Upper Byte:							
U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	OCSIDL	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
U-0	U-0	U-0	R-0, HC	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OCFLT	OCTSEL	OCM<2:0>		
bit 7							bit 0

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **OCSIDL:** Stop Output Compare in Idle Mode Control bit
1 = Output compare x will halt in CPU Idle mode
0 = Output compare x will continue to operate in CPU Idle mode

bit 12-5 **Unimplemented:** Read as '0'

bit 4 **OCFLT:** PWM Fault Condition Status bit
1 = PWM Fault condition has occurred (cleared in HW only)
0 = No PWM Fault condition has occurred
(This bit is only used when OCM<2:0> = 111.)

bit 3 **OCTSEL:** Output Compare Timer Select bit
1 = Timer3 is the clock source for compare x
0 = Timer2 is the clock source for compare x

Note: Refer to the device data sheet for specific time bases available to the output compare module.

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
111 = PWM mode on OCx, Fault pin enabled
110 = PWM mode on OCx, Fault pin disabled
101 = Initialize OCx pin low, generate continuous output pulses on OCx pin
100 = Initialize OCx pin low, generate single output pulse on OCx pin
011 = Compare event toggles OCx pin
010 = Initialize OCx pin high, compare event forces OCx pin low
001 = Initialize OCx pin low, compare event forces OCx pin high
000 = Output compare channel is disabled

Table 14-6: Example Register Map Associated with Output Compare Module

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TMR2	0106	Timer2 Register																0000 0000 0000 0000
TMR3	010A	Timer3 Register																0000 0000 0000 0000
PR2	010C	Period Register 2																1111 1111 1111 1111
PR3	010E	Period Register 3																1111 1111 1111 1111
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000 0000 0000 0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000 0000 0000 0000
OC1RS	0180	Output Compare 1 Secondary Register																uuuu uuuu uuuu uuuu
OC1R	0182	Output Compare 1 Register																uuuu uuuu uuuu uuuu
OC1CON	0184	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000 0000 0000 0000
OC2RS	0186	Output Compare 2 Secondary Register																uuuu uuuu uuuu uuuu
OC2R	0188	Output Compare 2 Register																uuuu uuuu uuuu uuuu
OC2CON	018A	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000 0000 0000 0000
OC3RS	018C	Output Compare 3 Secondary Register																uuuu uuuu uuuu uuuu
OC3R	018E	Output Compare 3 Register																uuuu uuuu uuuu uuuu
OC3CON	0190	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000 0000 0000 0000
OC4RS	0192	Output Compare 4 Secondary Register																uuuu uuuu uuuu uuuu
OC4R	0194	Output Compare 4 Register																uuuu uuuu uuuu uuuu
OC4CON	0196	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000 0000 0000 0000
OC5RS	0198	Output Compare 5 Secondary Register																uuuu uuuu uuuu uuuu
OC5R	019A	Output Compare 5 Register																uuuu uuuu uuuu uuuu
OC5CON	019C	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000 0000 0000 0000
OC6RS	019E	Output Compare 6 Secondary Register																uuuu uuuu uuuu uuuu
OC6R	01A0	Output Compare 6 Register																uuuu uuuu uuuu uuuu
OC6CON	01A2	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000 0000 0000 0000
OC7RS	01A4	Output Compare 7 Secondary Register																uuuu uuuu uuuu uuuu
OC7R	01A6	Output Compare 7 Register																uuuu uuuu uuuu uuuu
OC7CON	01A8	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000 0000 0000 0000
OC8RS	01AA	Output Compare 8 Secondary Register																uuuu uuuu uuuu uuuu
OC8R	01AC	Output Compare 8 Register																uuuu uuuu uuuu uuuu
OC8CON	01AE	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000 0000 0000 0000
IFS0	0084	CNIF	MI2CIF	SI2CIF	NVMIF	ADIF	U1TXIF	U1RXIF	SPI1IF	T3IF	T2IF	OC2IF	IC2IF	T1IF	OC1IF	IC1IF	INT0	0000 0000 0000 0000
IFS1	0086	IC6IF	IC5IF	IC4IF	IC3IF	C1IF	SPI2IF	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	IC8IF	IC7IF	INT1IF	0000 0000 0000 0000
IFS2	0088	—	—	—	FLTBIF	FLTAIF	LVDIF	DCIIF	QEIIF	PWMIF	C2IF	INT4IF	INT3IF	OC8IF	OC7IF	OC6IF	OC5IF	0000 0000 0000 0000
IEC0	008C	CNIE	MI2CIE	SI2CIE	NVMIE	ADIE	U1TXIE	U1RXIE	SPI1IE	T3IE	T2IE	OC2IE	IC2IE	T1IE	OC1IE	IC1IE	INT0IE	0000 0000 0000 0000
IEC1	008E	IC6IE	IC5IE	IC4IE	IC3IE	C1IE	SPI2IE	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	IC8IE	IC7IE	INT1IE	0000 0000 0000 0000
IEC2	0090	—	—	—	FLTBIE	FLTAIE	LVDIE	DCIIE	QEIIE	PWMIE	C2IE	INT4IE	INT3IE	OC8IE	OC7IE	OC6IE	OC5IE	0000 0000 0000 0000
IPC0	0094	—	T1IP<2:0>		—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>				0100 0100 0100 0100
IPC1	0096	—	T3IP<2:0>		—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>				0100 0100 0100 0100
IPC4	009C	—	OC3IP<2:0>		—	IC8IP<2:0>			—	IC7IP<2:0>			—	INT1IP<2:0>				0100 0100 0100 0100
IPC5	009E	—	INT2IP<2:0>		—	T5IP<2:0>			—	T4IP<2:0>			—	OC4IP<2:0>				0100 0100 0100 0100
IPC8	00A4	—	OC8IP<2:0>		—	OC7IP<2:0>			—	OC6IP<2:0>			—	OC5IP<2:0>				0100 0100 0100 0100

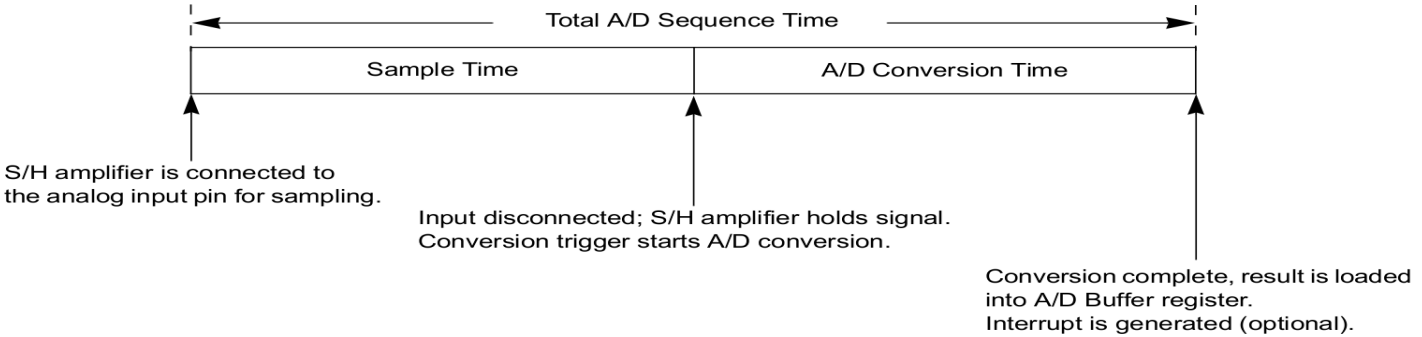
Legend: u = uninitialized

Note: The register map will depend on the number of output compare modules on the device. Please refer to the device data sheet for details.

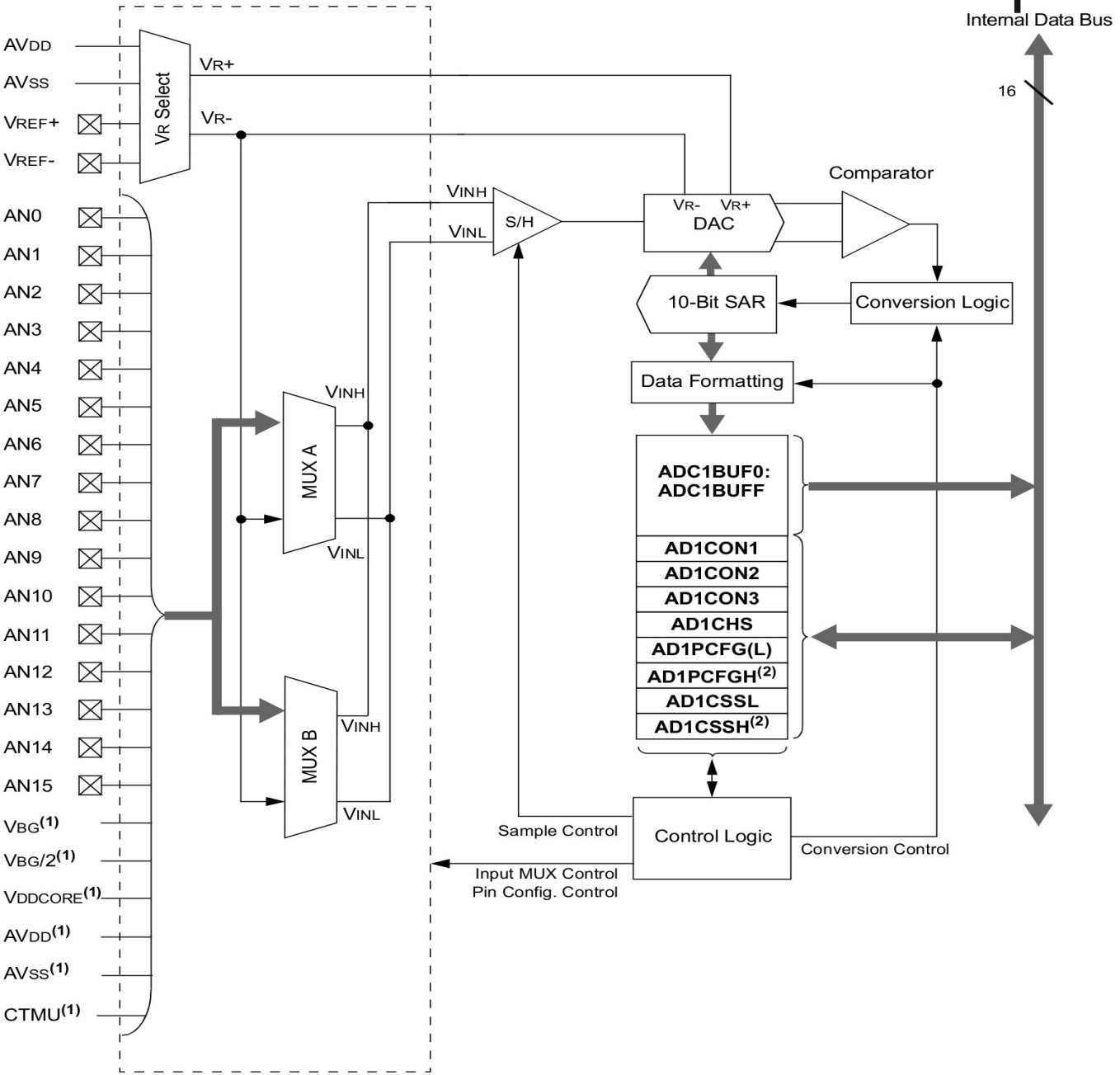
- Modos de comparación (seleccionado por OCM<2:0>)
  - Modo comparación simple → compara con el registro OCxR
    - OCM<2:0>=001 → inicializa el pin OCx a 0, la comparación pone el pin a 1
    - OCM<2:0>=010 → inicializa el pin OCx a 1, la comparación pone el pin a 0
    - OCM<2:0>=011 → cada evento de comparación conmuta el pin OCx
  - Modo de comparación doble → compara con los registros OCxR y OCxRS
    - Salida de pulso simple (OCM<2:0>=100)
      - El pin se inicializa a 0
      - Cuando el TMR coincide con OCxR el pin se pone a 1
      - Cuando el TMR coincide con OCxRS el pin se pone a 0
      - El pin continuará a 0 hasta que se cambia de modo o se deshabilita el módulo
    - Salida de pulso continuo (OCM<2:0>=101)
      - El pin se inicializa a 0
      - Cuando el TMR coincide con OCxR el pin se pone a 1
      - Cuando el TMR coincide con OCxRS el pin se pone a 0
      - Continúa haciendo transiciones en las siguientes coincidencias con los registros.

ADC 10/12 bits

- Todos los modelos tienen un ADC de 10 bits
- Hasta 16 entradas analógicas (hasta 32 en los dsPIC33)
- Velocidades de conversión de hasta 500Msps-1100Msps (según dispositivo)
- En algunos el ADC puede funcionar además con 12 bits (en los PIC24F no)
- En algunos modelos, el ADC de 10 bits (nunca el de 12) puede muestrear 4 señales a la vez (es un ADC único pero con 4 S&H).
- Buffer FIFO de 16 muestras. Algunos dsPIC33 y PIC24H tienen DMA.
- Algunos (pocos) dispositivos tienen posibilidad de tensión de referencia interna
- Posibilidad de entradas con referencia a tierra o diferenciales
- A diferencia de la conversión A/D en los PIC de 8 bits, el muestreo y la conversión se controlan de forma separada (distintos bits en los registros de control)



ADC de 10 bits con muestreo simple



Note 1: Internal analog channels are implemented in select devices only. Different device families implement different combinations of channels. Refer to the specific device data sheet for details.

2: Implemented in select devices only.

Register 17-1: AD1CON1: A/D Control Register 1

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
ADON	—	ADSIDL	—	—	—	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0, HCS	R/C-0, HCS
SSRC2	SSRC1	SSRC0	—	—	ASAM	SAMP	DONE
bit 7							bit 0

Legend:	C = Clearable bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HCS = Hardware Clearable/Settable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADON:** A/D Operating Mode bit
1 = A/D Converter module is operating
0 = A/D Converter is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 **FORM<1:0>:** Data Output Format bits
11 = Signed fractional (sddd dddd dd00 0000) → Resultado -0,5/0,499 (formato S1.15)
10 = Fractional (dddd dddd dd00 0000) → Resultado 0/0,999 (formato 1.15)
01 = Signed integer (ssss sssd dddd dddd) → Resultado -512/+511
00 = Integer (0000 00dd dddd dddd) → Resultado 0/1023

bit 7-5 **SSRC<2:0>:** Conversion Trigger Source Select bits (event ends sampling and starts conversion)
111 = Internal counter (auto-convert)
110 = CTMU event (when not implemented as '100')(1)
101 = Reserved
100 = CTMU event(1)
011 = Timer5 compare match(1,2)
010 = Timer3 compare match(2)
001 = Active transition on INT0 pin (basic sync convert)
000 = Clearing SAMP bit (full program control)

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** A/D Sample Auto-Start Mode bit
1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** A/D Sample Enable Mode Mode bit
1 = A/D Sample-and-Hold amplifier is sampling
0 = A/D Sample-and-Hold amplifier is holding
When ASAM = 0, writing '1' to this bit starts sampling. When SSRC<2:0> = 000, writing '0' to this bit will end sampling and start conversion.

bit 0 **DONE:** A/D Conversion Status bit
1 = A/D conversion is done
0 = A/D conversion is not done or has not started
Clearing this bit will not affect any operation in progress; it is cleared by software or start of a new conversion.

Note 1: This option is available in select devices only. Refer to the specific device data sheet.
2: Use Timer3 or Timer5 as a clock divider for a fixed sample rate. The T3CK or T5CK input may also be selected with this mode to synchronize with an external event by configuring the counter to clock from the T3CK pin while preset for one pulse. See **Section 14. "Timers"** for more information.

Register 17-2: AD1CON2: A/D Control Register 2

R/W-0	R/W-0	R/W-0	r-0	U-0	R/W-0	U-0	U-0
VCFG2	VCFG1	VCFG0	r	—	CSCNA	—	—
bit 15							bit 8

R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS(1)	—	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

VCFG<2:0>	VR+	VR-
000	AVDD	AVSS
001	External VREF+ Pin	AVSS
010	AVDD	External VREF- Pin
011	External VREF+ Pin	External VREF- Pin
1xx	AVDD	AVSS

bit 12 **Reserved:** Maintain as '0'

bit 11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** MUX A Channel Scan/Input Channel Select bit
1 = Scan inputs selected by the AD1CSSL register as the MUX A input
0 = Use the channel selected by the CH0SA bits as the MUX A input

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit(1)
1 = A/D is currently filling ADC1BUF8-ADC1BUFF, user should access data in ADC1BUF0-ADC1BUF7
0 = A/D is currently filling ADC1BUF0-ADC1BUF7, user should access data in ADC1BUF8-ADC1BUFF

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits
1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
.....
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** Buffer Mode Select bit
1 = Buffer configured as two 8-word buffers (ADC1BUF0 to ADC1BUF7 and ADC1BUF8 to ADC1BUFF)
0 = Buffer configured as one 16-word buffer (ADC1BUF0 to ADC1BUFF)

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Alternate between MUX A and MUX B input multiplexer settings on successive conversions, starting with MUX A
0 = Always uses MUX A input multiplexer settings

Note 1: Only valid when ADC1BUF is functioning as two buffers (BUFM = 1).

Register 17-3: AD1CON3: A/D Control Register 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADRC:** A/D Conversion Clock Source bit
1 = A/D internal RC clock
0 = Clock derived from system clock

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits
11111 = 31 TAD
.....
00001 = 1 TAD
00000 = 0 TAD (not recommended)

bit 7-0 **ADCS<7:0>:** A/D Conversion Clock Period Select bits(1)
11111111
..... = Reserved
01000000

00111111 = 64 • Tcy
.....
00000001 = 2 • TCY
00000000 = TCY

Note 1: Only valid when using the system clock as the conversion clock (ADRC = 0).

Register 17-4: AD1CHS: A/D Input Channel Select Register

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	—	CH0SB4(1)	CH0SB3	CH0SB2	CH0SB1	CH0SB0
bit 15							bit 8

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	—	—	CH0SA4(1)	CH0SA3	CH0SA2	CH0SA1	CH0SA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CH0NB:** S/H Amplifier Negative Input Select for MUX B Multiplexer Setting bit
1 = Negative input is AN1
0 = Negative input is VR-

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **CH0SB<4:0>:** S/H Amplifier Positive Input Select for MUX B Multiplexer Setting bits(1)
The number of implemented analog inputs and the bit combinations assigned to them vary significantly between device families. In general, external analog inputs, AN0 through AN15 (where implemented), are sequentially assigned from '00000' as shown below. If a sequential input is unimplemented, its corresponding bit value is also unimplemented.
In addition, some devices implement inputs for internal band gap references, external voltage references, and other analog modules, such as the CTMU. Refer to the specific device data sheet for a complete listing of implemented inputs for a particular device.
Any bit combinations not explicitly listed are unimplemented. Using an unimplemented channel for a conversion will produce unpredictable results.
01111 = Positive input is AN15
01110 = Positive input is AN14
01101 = Positive input is AN13
01100 = Positive input is AN12
01011 = Positive input is AN11
01010 = Positive input is AN10
01001 = Positive input is AN9
01000 = Positive input is AN8
00111 = Positive input is AN7
00110 = Positive input is AN6
00101 = Positive input is AN5
00100 = Positive input is AN4
00011 = Positive input is AN3
00010 = Positive input is AN2
00001 = Positive input is AN1
00000 = Positive input is AN0

bit 7 **CH0NA:** S/H Amplifier Negative Input Select for MUX A Multiplexer Setting bit
1 = Negative input is AN1
0 = Negative input is VR-

bit 6-5 **Unimplemented:** Read as '0'

bit 4-0 **CH0SA<4:0>:** S/H Amplifier Positive Input Select for MUX A Multiplexer Setting bits(1)
Implemented combinations are identical to those for CH0SB<4:0>.

Note 1: CH0SB4 and CH0SA4 are implemented in select devices only. Their implementation generally indicates an extended range of input sources from voltage references and other analog modules.

Register 17-5: AD1PCFG(L): A/D Port Configuration Low Register(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PCFG<15:0>:** Analog Input Pin Configuration Control bits

1 = Pin for corresponding analog channel is in Digital mode; port read input enabled, A/D input multiplexer input connected to AVSS

0 = Pin for corresponding analog channel is in Analog mode; port read input disabled, A/D module samples pin voltage

Note 1: In devices without the internal band gap reference options, this register is named AD1PCFG. In devices with the band gap options, it is named AD1PCFGL.

Register 17-6: AD1PCFGH: A/D Port Configuration High Register(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	PCFG17	PCFG16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **PCFG17:** A/D Input Band Gap Scan Enable bit

1 = Analog channel disabled from input scan

0 = Internal band gap (VBG) channel enabled for A/D MUX input

bit 0 **PCFG16:** A/D Input Half Band Gap Scan Enable bit

1 = Analog channel disabled from input scan

0 = Internal VBG/2 channel enabled for A/D MUX input

Note 1: AD1PCFGH is implemented in select devices only.

Register 17-7: AD1CSSL: A/D Input Scan Select Low Register for MUX A(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CSSL<15:0>:** A/D Input Channel Scan Selection bits
1 = Corresponding analog channel, ANx, is selected for sequential scanning on MUX A
0 = Corresponding analog channel is ignored in sequential scanning

Note 1: Only MUX A supports scanning of input channels.

Register 17-8: AD1CSSH: A/D Input Scan Select High Register for MUX A(1,2)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CSSL17	CSSL16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **CSSL17:** A/D Input Band Gap Scan Selection bit
1 = Internal band gap (V_{BG}) channel is selected for sequential scanning on MUX A
0 = Analog channel is ignored in sequential scanning

bit 0 **CSSL16:** A/D Input Half Band Gap Scan Selection bit
1 = Internal $V_{BG}/2$ channel is selected for sequential scanning on MUX A
0 = Analog channel is ignored in sequential scanning

Note 1: Only MUX A supports scanning of input channels.
2: AD1CSSH is implemented in select devices only.

- Configuración de la interrupción
  - Seleccionar las tensiones de referencia → bits VCFG<2:0>
  - Seleccionar el reloj del ADC (T_{AD}) → bits ADRC y ADCS<7:0> (conversión en $12T_{AD}$)
  - Configurar pines analógicos → registro(s) AD1PCFG y TRIS
  - Determinar como ocurre el muestreo
    - Bit ALTS=1 → alterna MUX-A y MUX-B en cada muestreo
    - Bit CSCNA=1 → muestrea secuencialmente los canales indicados en AD1CSSL
  - Seleccionar el canal → CH0SA<3:0> y CH0SB<3:0>
  - Seleccionar la secuencia muestreo/conversión → bit ASAM muestreo automático/manual
  - Seleccionar el formato de los datos → bits FORM<1:0>
  - Seleccionar el número de lecturas por interrupción → bits SMPI<3:0>
  - Configurar la interrupción → ADIF, ADIE, GIE, prioridad
  - Activar el módulo A/D → ADON
- Adquisición de un dato
  - Con muestreo manual (ASAM=0)
    - Poner SAMP=1 inicia el muestreo
    - Poner SAMP=0 finaliza el muestreo y empieza la conversión
  - Con muestreo automático (ASAM=1)
    - El muestreo empieza automáticamente al terminar la conversión (SAMP=1 por HW)
    - La conversión se inicia cuando se pone SAMP=1 (por SW)
  - Disparo automático → SAMC<4:0> nº de T_{AD} antes de re-disparar → combinado con ASAM=1 hace que el ADC “funcione solo”

Table 17-4: ADC Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	ADC Data Buffer 0																xxxx
ADC1BUF1	ADC Data Buffer 1																xxxx
ADC1BUF2	ADC Data Buffer 2																xxxx
ADC1BUF3	ADC Data Buffer 3																xxxx
ADC1BUF4	ADC Data Buffer 4																xxxx
ADC1BUF5	ADC Data Buffer 5																xxxx
ADC1BUF6	ADC Data Buffer 6																xxxx
ADC1BUF7	ADC Data Buffer 7																xxxx
ADC1BUF8	ADC Data Buffer 8																xxxx
ADC1BUF9	ADC Data Buffer 9																xxxx
ADC1BUFA	ADC Data Buffer 10																xxxx
ADC1BUFB	ADC Data Buffer 11																xxxx
ADC1BUFC	ADC Data Buffer 12																xxxx
ADC1BUFD	ADC Data Buffer 13																xxxx
ADC1BUFE	ADC Data Buffer 14																xxxx
ADC1BUFF	ADC Data Buffer 15																xxxx
AD1CON1	ADON	—	ADSIDL	—	—	—	FORM1	FORM0	SSRC2	SSRC1	SSRC0	—	—	ASAM	SAMP	DONE	0000
AD1CON2	VCFG2	VCFG1	VCFG0	r	—	CSCNA	—	—	BUFS	—	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CON3	ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CHS	CH0NB	—	—	CH0SB4(2)	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA	—	—	CH0SA4(2)	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1PCFGL(1)	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
AD1PCFGH(2)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PCFG17	PCFG16	0000
AD1CSSL	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
AD1CSSH(2)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CSSL17	CSSL16	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is named AD1PCFG in devices without the AD1PCFGH register.

2: These registers and/or bits are implemented in select devices only.

Documentación

- Pic24F Family Reference Manual (un PDF por sección)
  - http://www.microchip.com/stellent/idcplg?IdcService=SS_GET_PAGE&nodeId=2575
- PIC24H Family Reference Manual (un PDF por sección)
  - http://www.microchip.com/stellent/idcplg?IdcService=SS_GET_PAGE&nodeId=2572
- dsPIC33F Family Reference Manual (un PDF por sección)
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