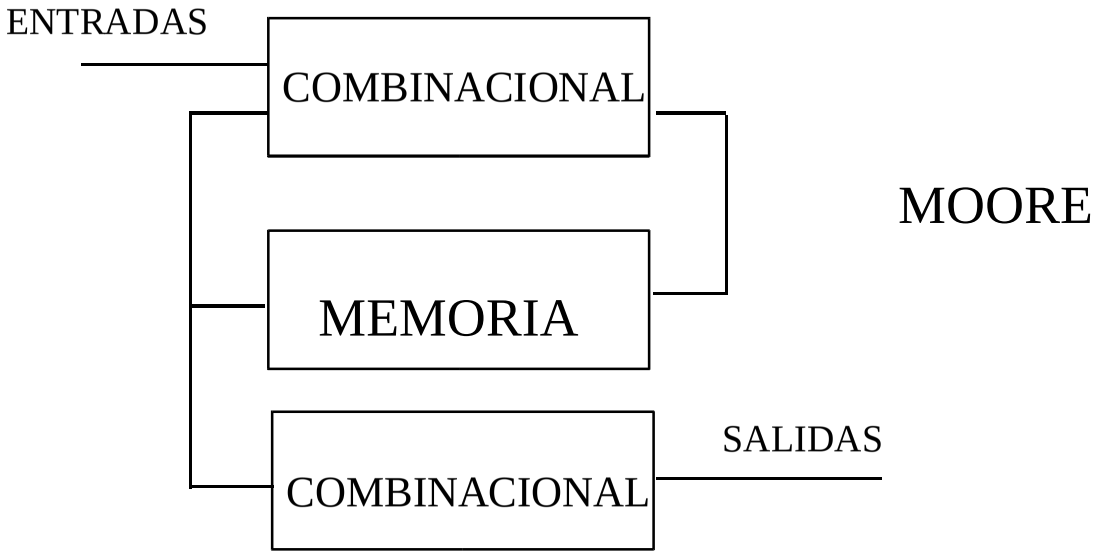
Circuitos secuenciales

MEALY

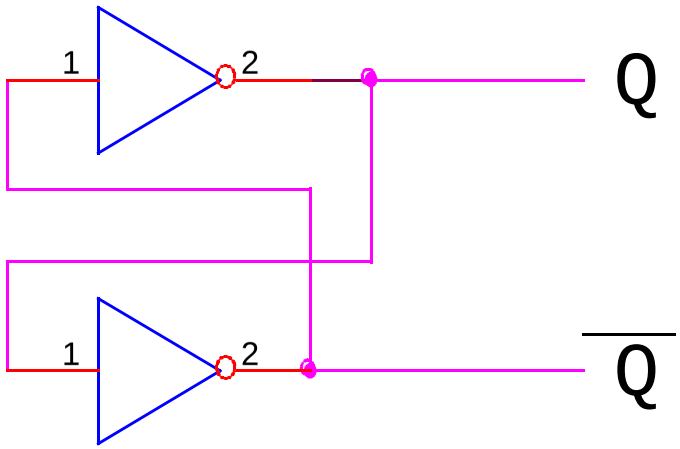


MOORE

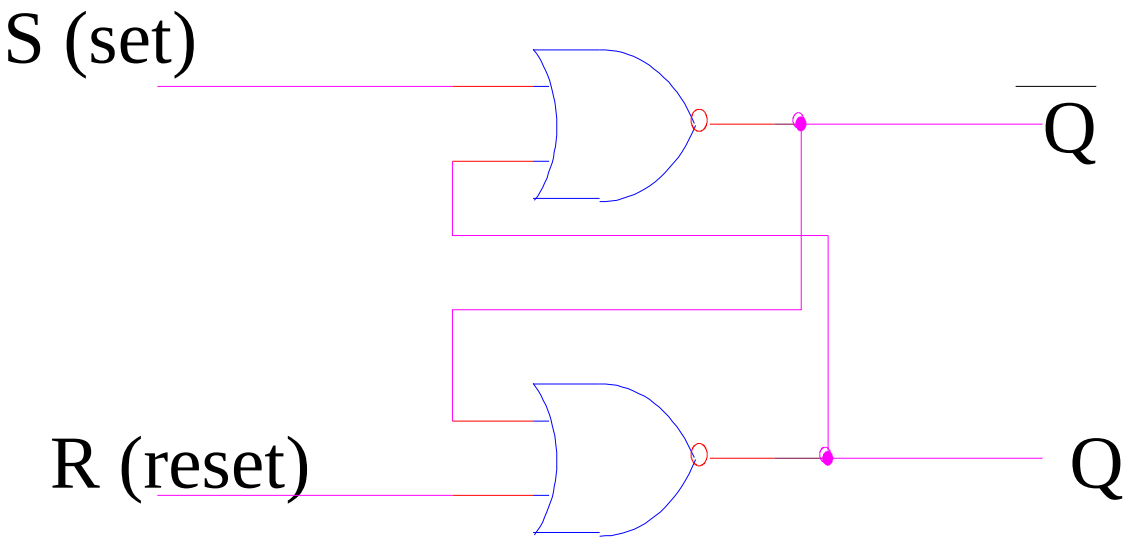
CLASIFICACIÓN

- Según la estructura
  - » Moore
  - » Mealy
- Según la evolución
  - » Síncronos
    - Por nivel
    - Por flanco
  - » Asíncronos

Elemento de memoria con dos inversores

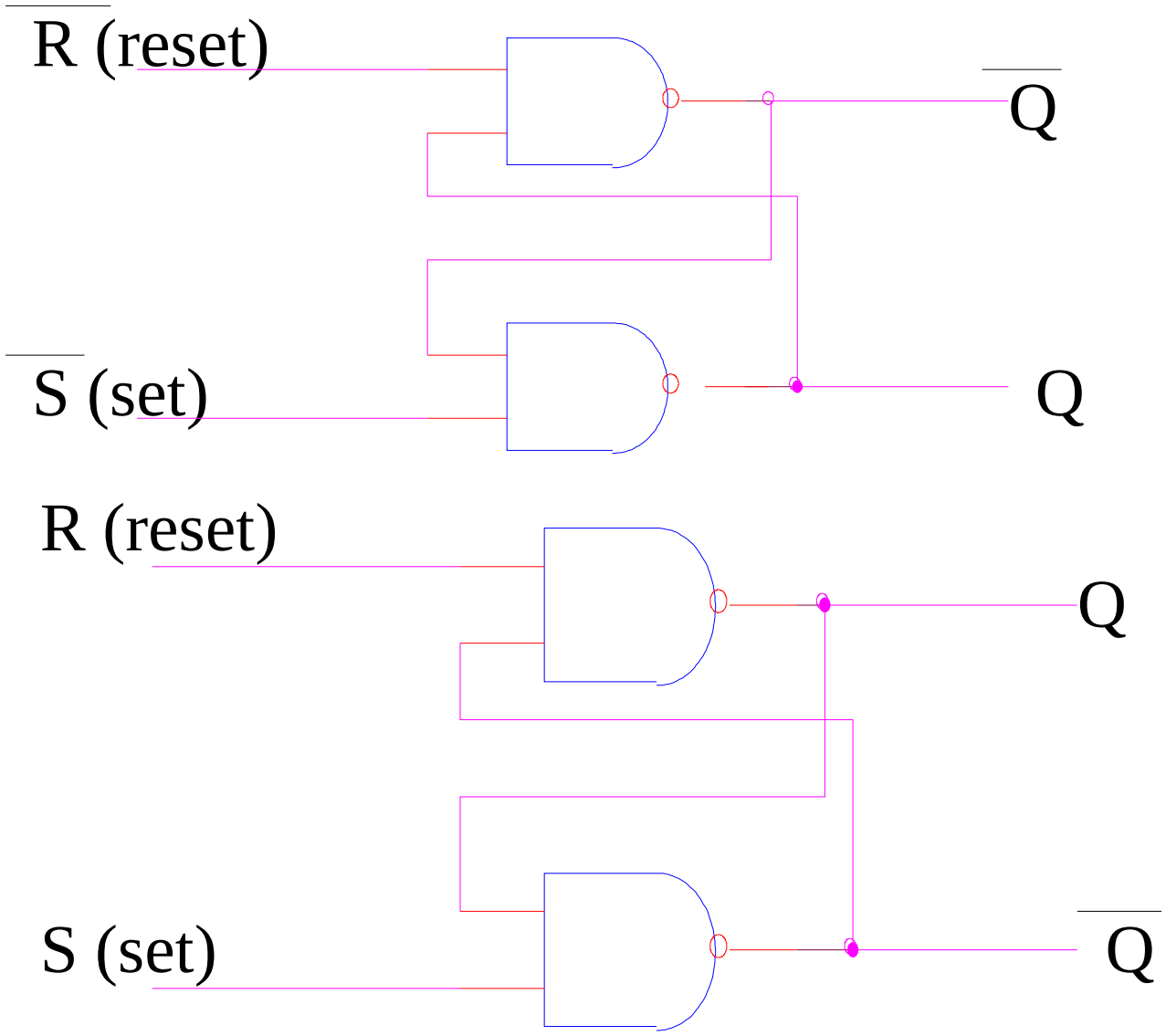


Biestable SR con puertas NOR

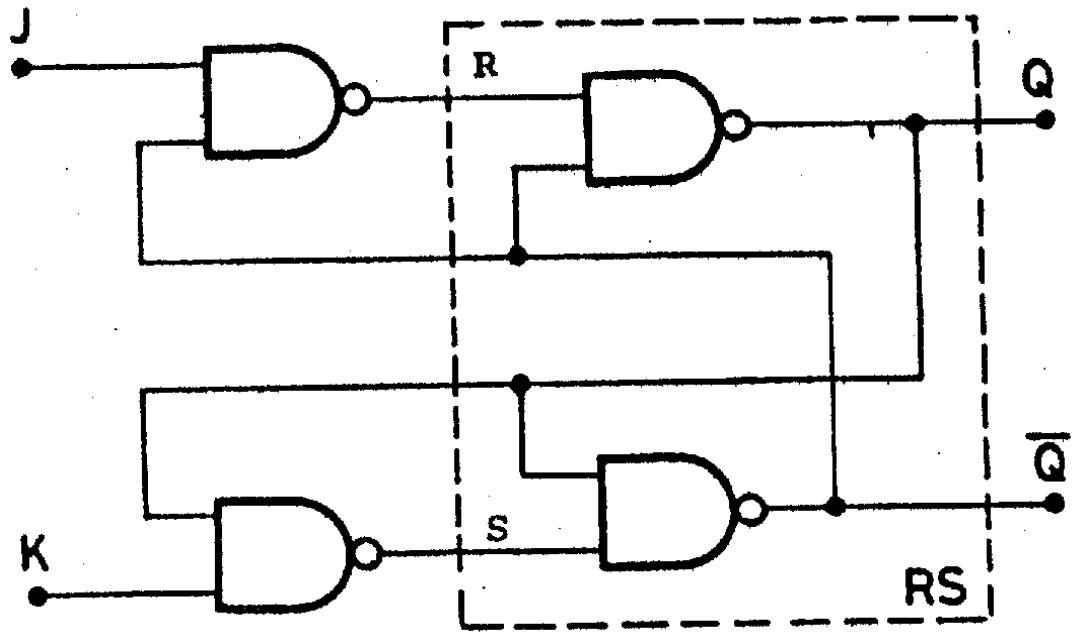


S	R	Q(t+1)
0	0	No cambia
0	1	0
1	0	1
1	1	No usada

Biestables RS

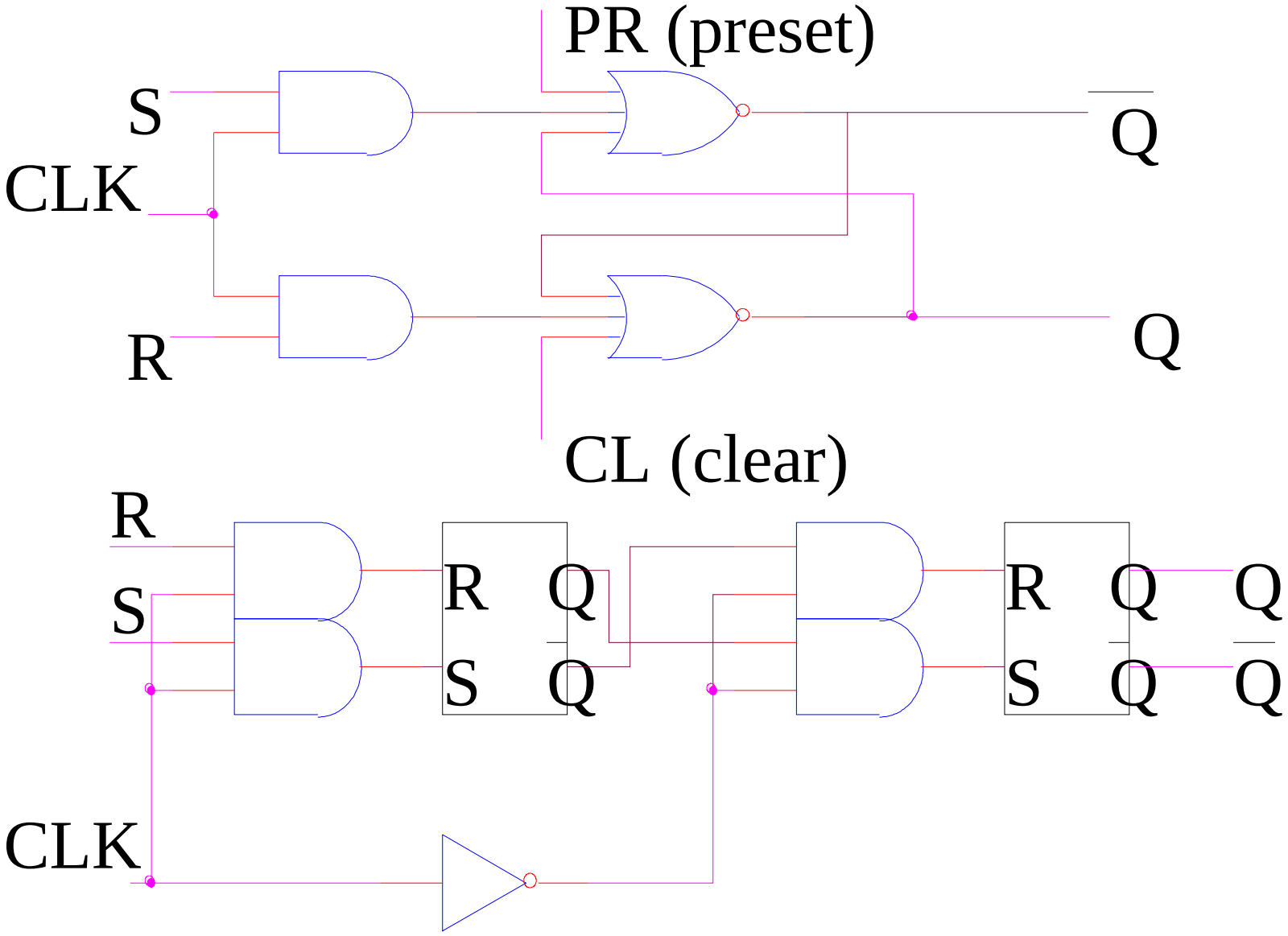


Biestable JK

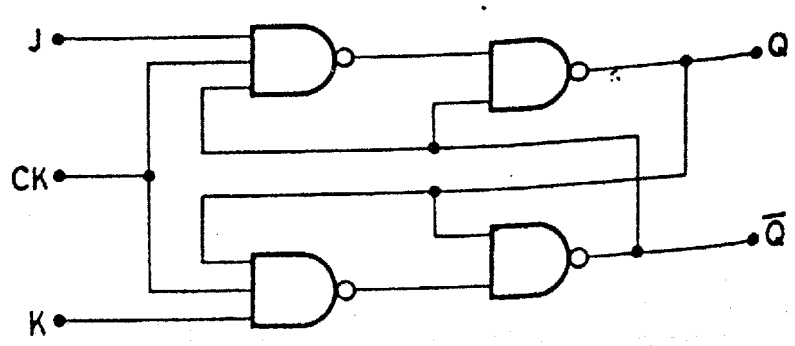


J	K	Q_{t-1}	Q_t	
0	0	0 1	Q_{t-1}	no cambia
1	0	0 1	1	se pone a 1
0	1	0 1	0	se pone a 0
1	1	0 1	$\bar{Q}_{t-1}$	siempre cambia

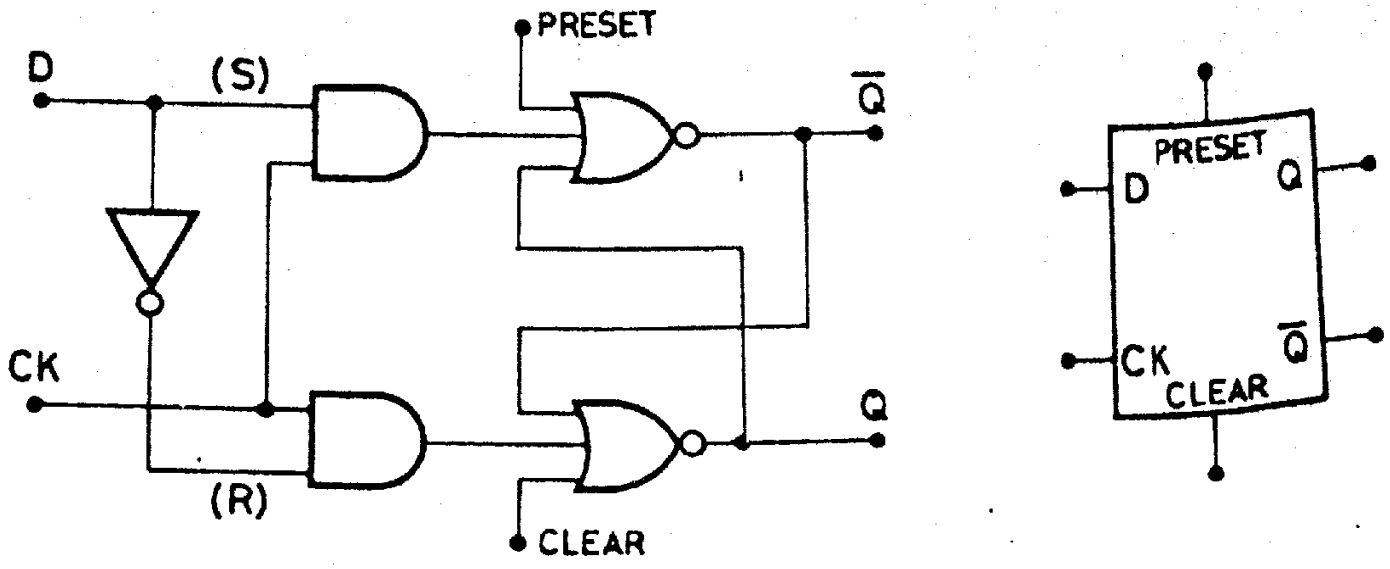
RS con PR y CL y flip−flop master−slave



BIESTABLE JK LATCH SÍNCRONO



BIESTABLE D LATCH SÍNCRONO



Flip-flop S-R disparado por flanco de subida

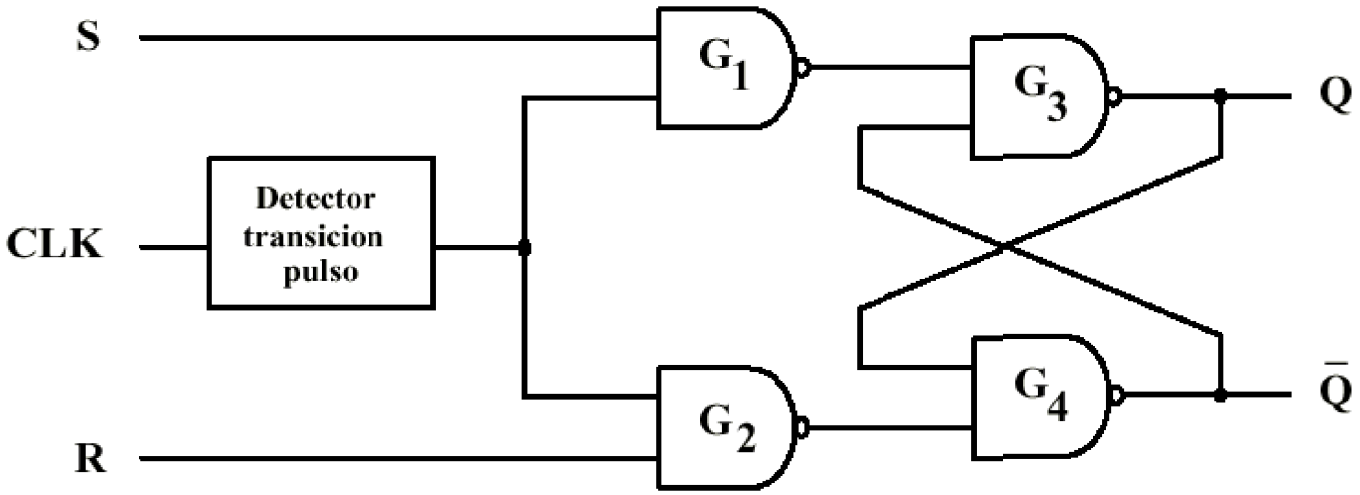


Tabla de verdad

Entradas			Salidas		Comentarios
S	R	CLK	Q	/Q	
0	0	X	Q_0	$/Q_0$	No cambia
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Condición no válida

Símbolo

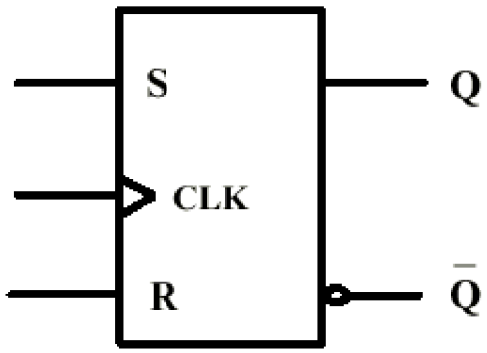
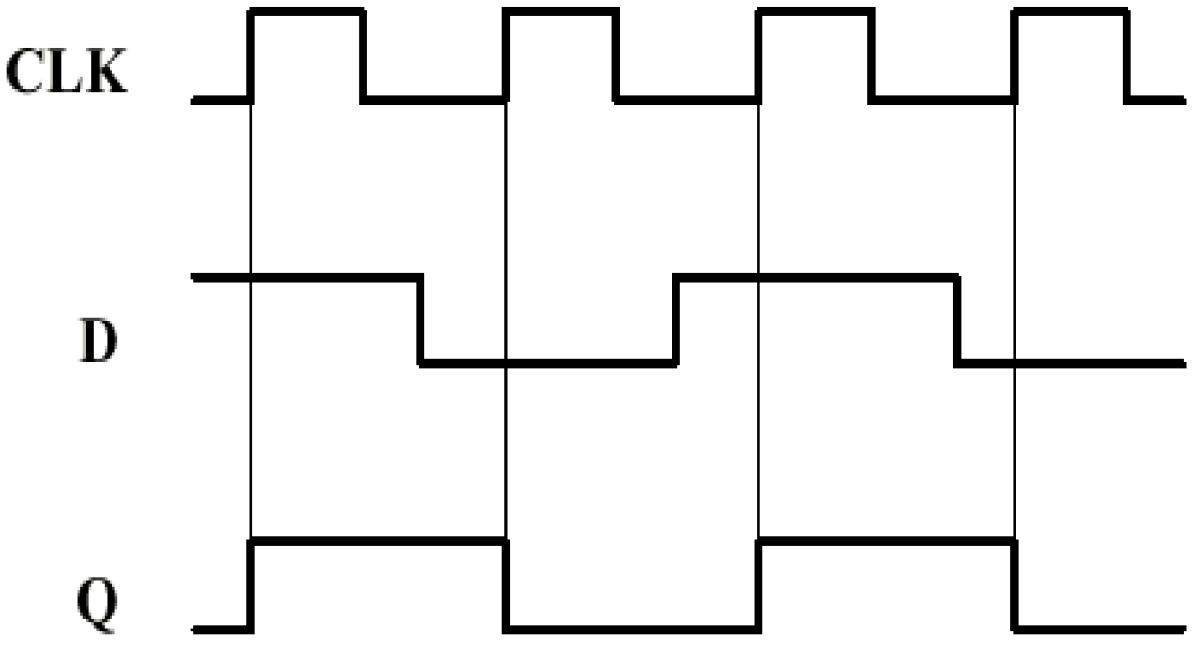


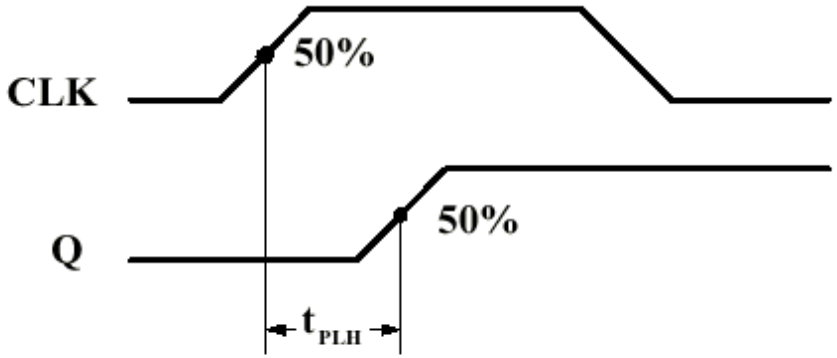
Tabla de verdad de un flip-flop D disparado por flanco de subida

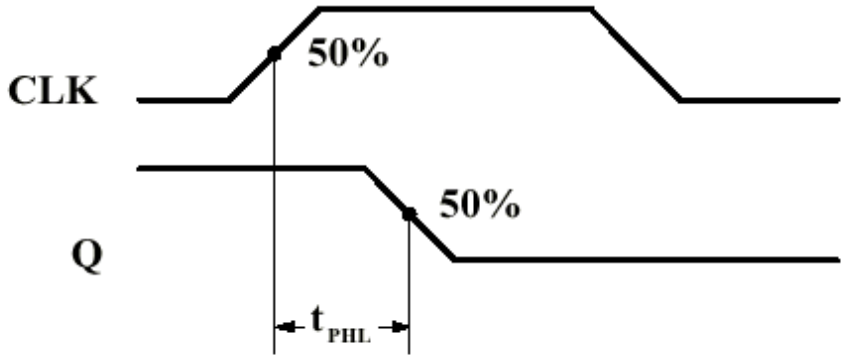
Entradas		Salidas		Comentarios
D	CLK	Q	/Q	
1	↑	1	0	SET
0	↑	0	1	RESET

Ejemplo

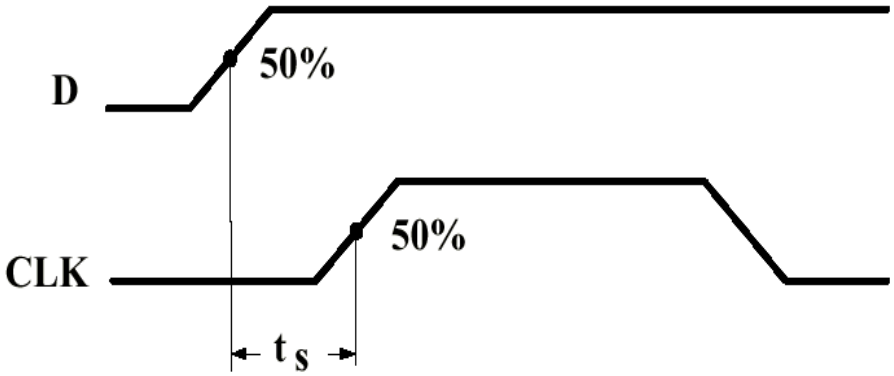


Tiempos de propagación

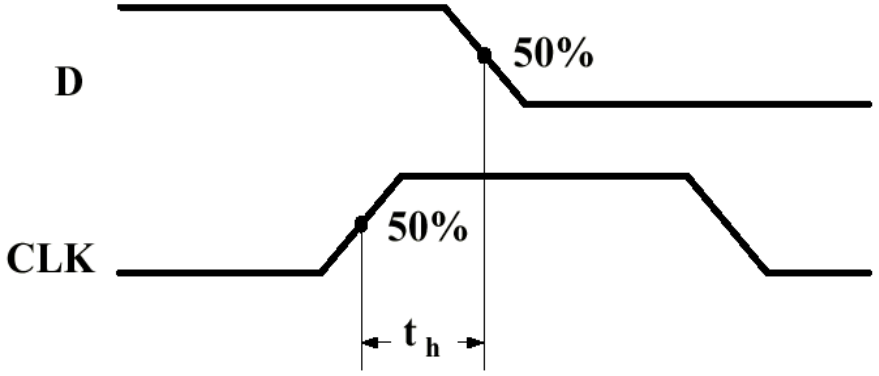




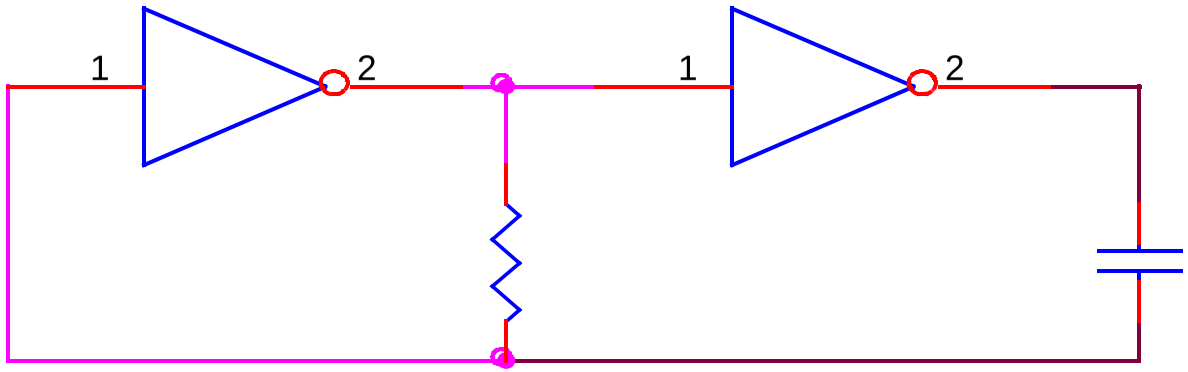
Tiempo de *set-up*

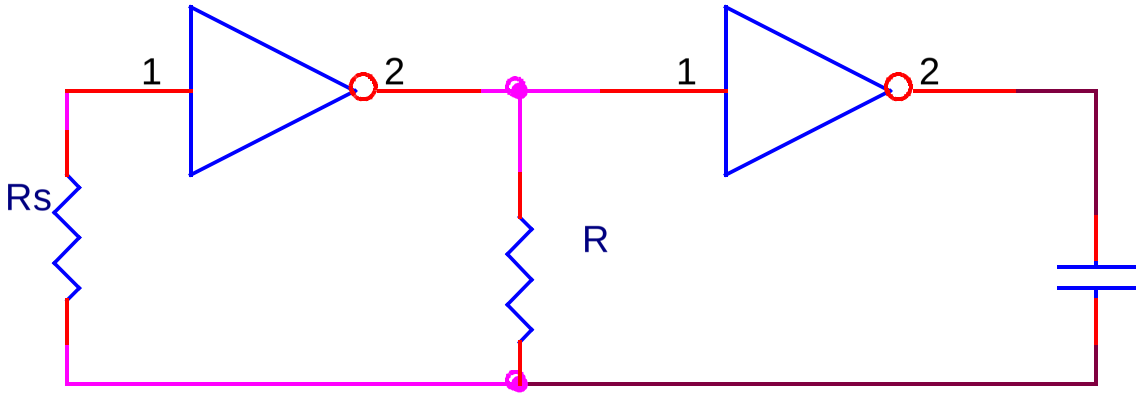


Tiempo de *hold*

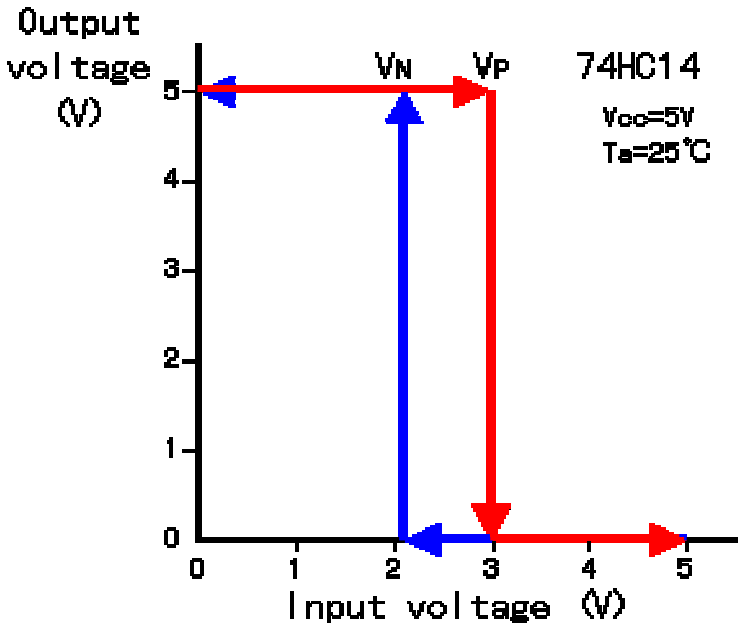


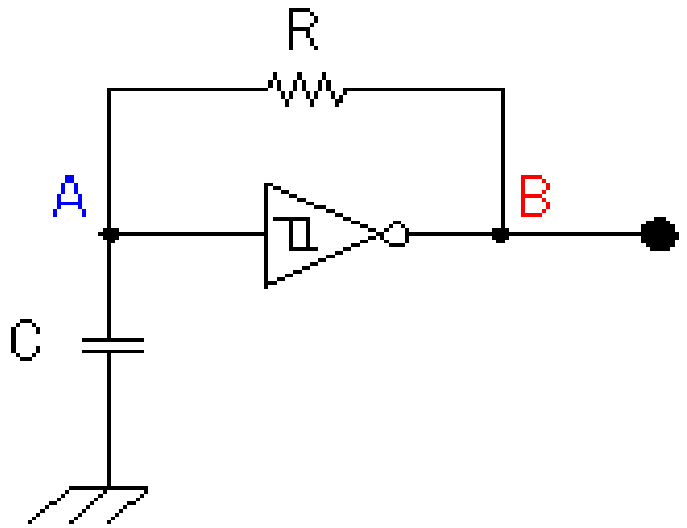
Aestables



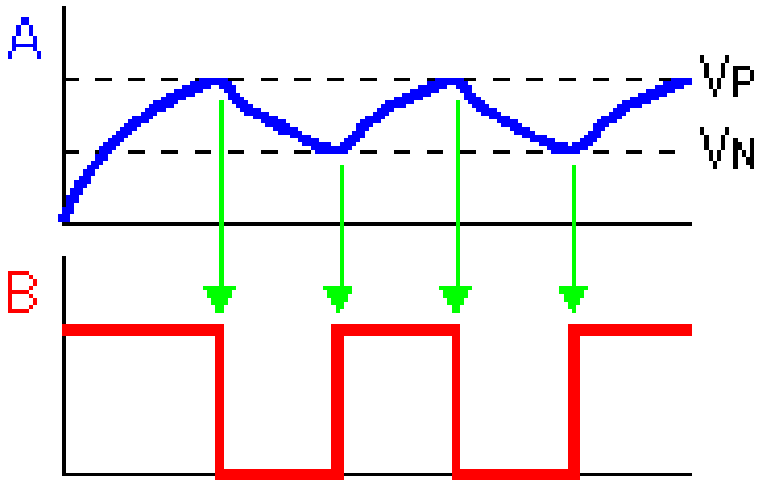


Aestable con negador trigger schmitt

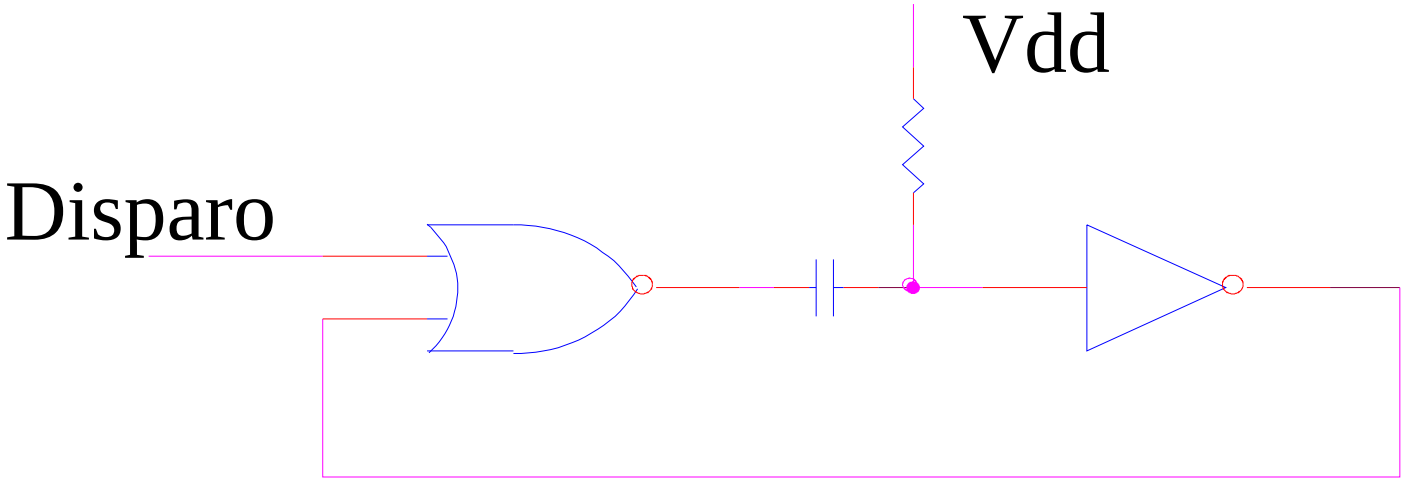


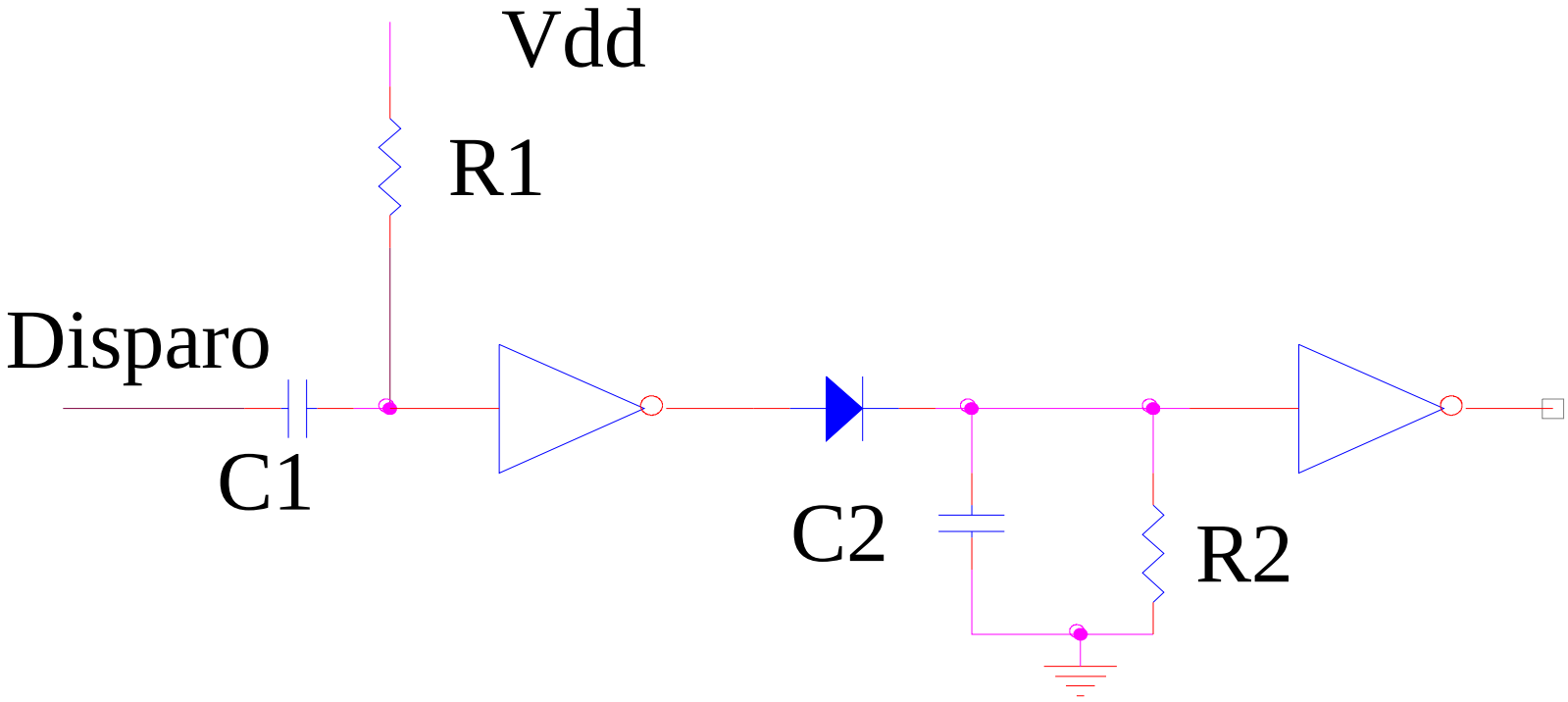


T=1’2 RC

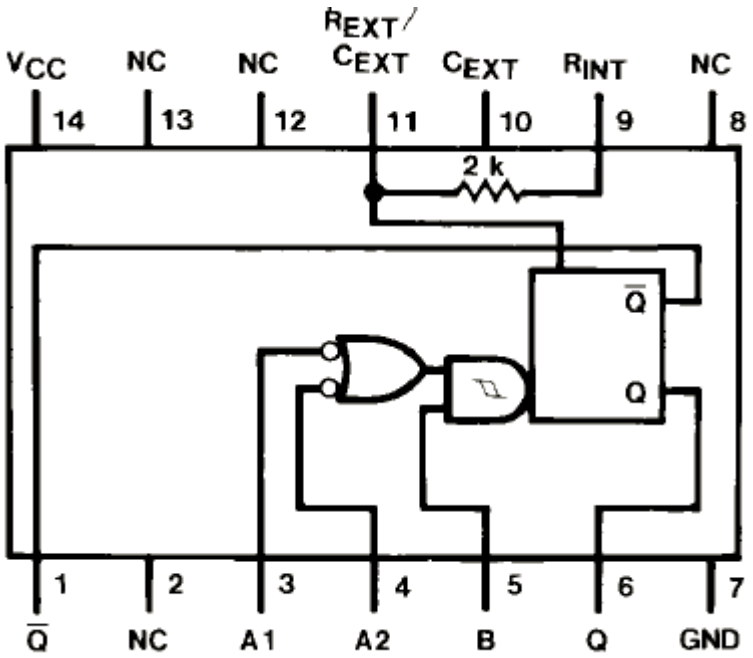


Monoestables





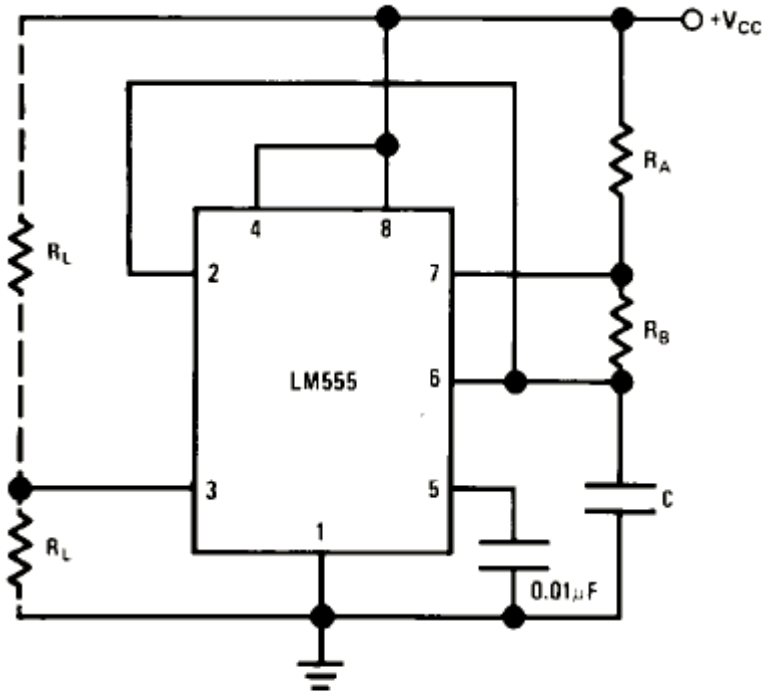
Monoestable con 74121



Function Table

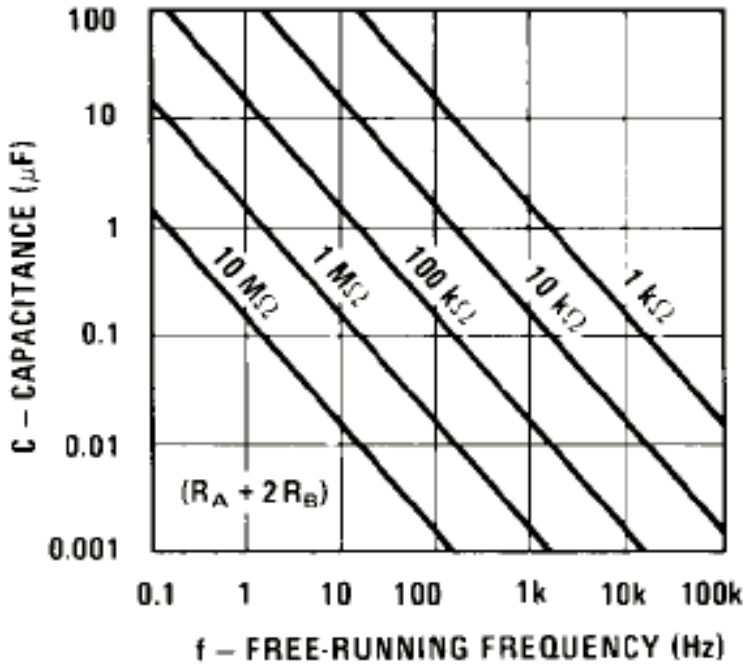
Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

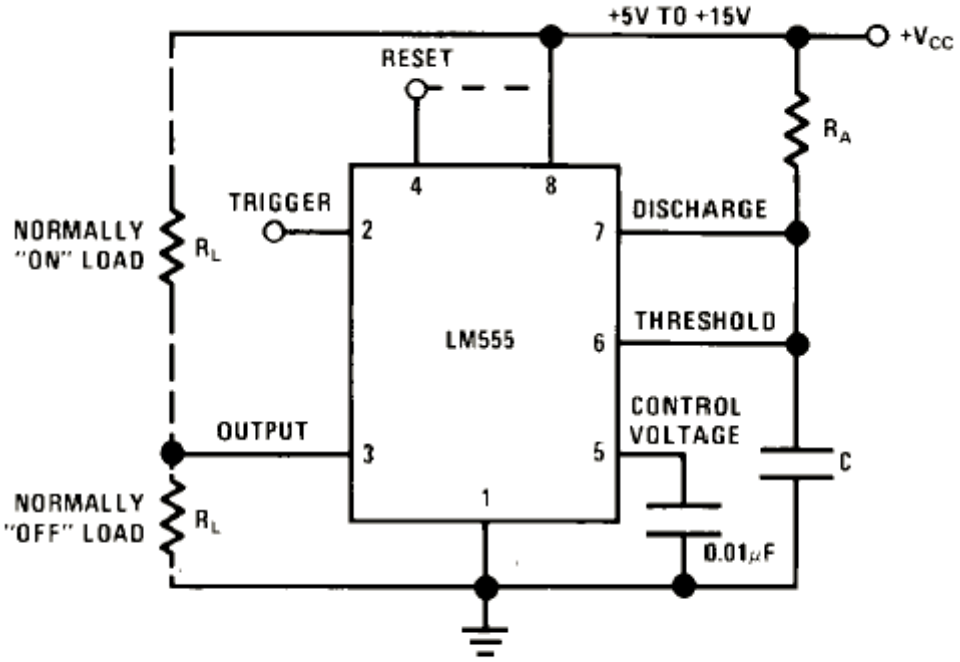
Aestables y monoestables con LM55



DS0078

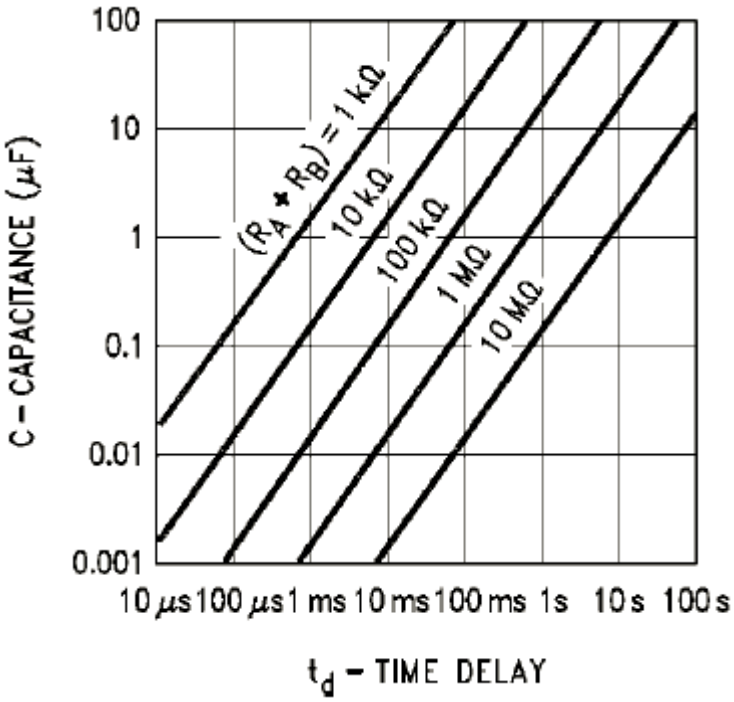
FIGURE 4. Astable

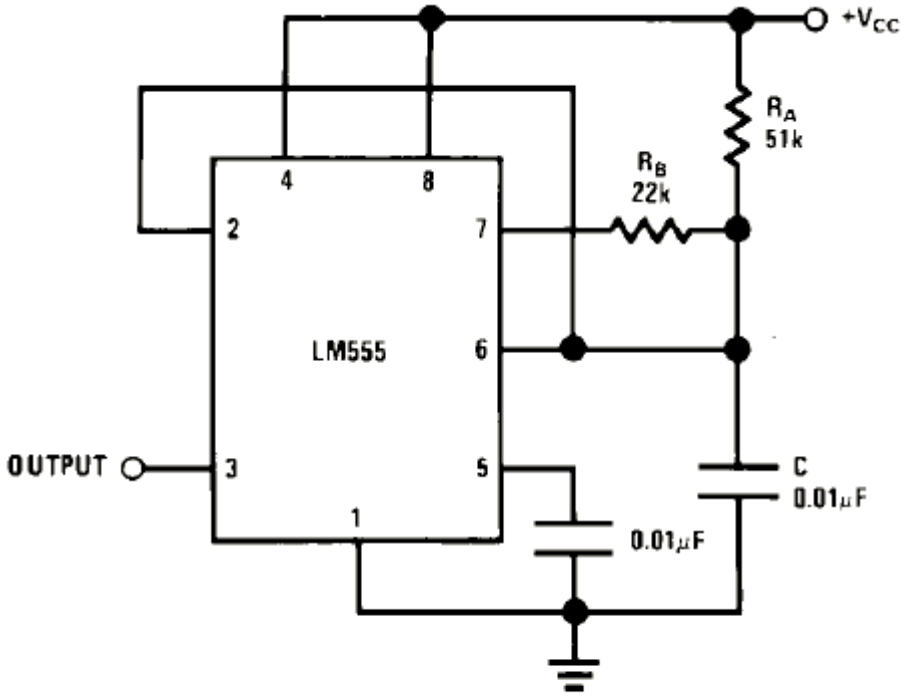




DS007851-5

FIGURE 1. Monostable





DS007851-18

FIGURE 14. 50% Duty Cycle Oscillator

National Semiconductor

June 1989

54121/DM54121/DM74121 One-Shot with Clear and Complementary Outputs

General Description

The DM54/74121 is a monostable multivibrator featuring both positive and negative edge triggering with complementary outputs. An internal 2kΩ timing resistor is provided for design convenience minimizing component count and layout problems. This device can be used with a single external capacitor. Inputs (A) are active-low trigger transition inputs and input (B) is an active-high transition Schmitt-trigger input that allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second. A high immunity to V_{CC} noise of typically 1.5V is also provided by internal circuitry at the input stage.

To obtain optimum and trouble free operation please read operating rules and NSC one-shot application notes carefully and observe recommendations.

Features

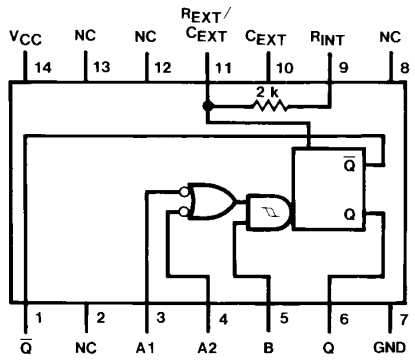
- Triggered from active-high transition or active-low transition inputs
- Variable pulse width from 30 ns to 28 seconds
- Jitter free Schmitt-trigger input
- Excellent noise immunity typically 1.2V
- Stable pulse width up to 90% duty cycle
- TTL, DTL compatible
- Compensated for V_{CC} and temperature variations
- Input clamp diodes
- Alternate Military/Aerospace device (54121) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Functional Description

The basic output pulse width is determined by selection of an internal resistor R_{INT} or an external resistor (R_X) and capacitor (C_X). Once triggered the output pulse width is independent of further transitions of the inputs and is a function of the timing components. Pulse width can vary from a few nano-seconds to 28 seconds by choosing appropriate R_X and C_X combinations. There are three trigger inputs from the device, two negative edge-triggering (A) inputs, one positive edge Schmitt-triggering (B) input.

Connection Diagram

Dual-In-Line Package



TL/F/6538–1

Order Number 54121DMQB, 54121FMQB, DM54121J, DM54121W or DM74121N
See NS Package Number J14A, N14A or W14B

Function Table

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⎍ = A Positive Pulse
⎎ = A Negative Pulse

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54121			DM74121			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage at the A Input (V_{CC} = Min)		1.4	2		1.4	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the A Input (V_{CC} = Min)	0.8	1.4		0.8	1.4		V
V_{T+}	Positive-Going Input Threshold Voltage at the B Input (V_{CC} = Min)		1.5	2		1.5	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the B Input (V_{CC} = Min)	0.8	1.3		0.8	1.3		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
t_W	Input Pulse Width (Note 1)	40			40			ns
dV/dt	Rate of Rise or Fall of Schmidt Input (B) (Note 1)			1			1	V/s
dV/dt	Rate of Rise or Fall of Logic Input (A) (Note 1)			1			1	V/μs
R_{EXT}	External Timing Resistor (Note 1)	1.4		30	1.4		40	kΩ
C_{EXT}	External Timing Capacitance (Note 1)	0		1000	0		1000	μF
DC	Duty Cycle (Note 1) R_T = 2 kΩ			67			67	%
	Duty Cycle (Note 1) $R_T = R_{EXT}$ (Max)			90			90	%
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	A1, A2			40	μA
			B			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A1, A2			−1.6	mA
			B			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	mA
I_{CC}	Supply Current	V_{CC} = Max	Quiescent		13	25	mA
			Triggered		23	40	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Outout Load)

Symbol	Parameter	From (Input) To (Output)	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	A1, A2 to Q	C_{EXT} = 80 pF, R_{INT} to V_{CC}, C_L = 15 pF, R_L = 400Ω		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q			55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A1, A2 to $\overline{Q}$			80	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$			65	ns
$t_{W(OUT)}$	Output Pulse Width Using the Internal Timing Resistor	A1, A2 or B to Q, $\overline{Q}$	C_{EXT} = 80 pF, R_{INT} to V_{CC}, R_L = 400Ω, C_L = 15 pF	70	150	ns
$t_{W(OUT)}$	Output Pulse Width Using Zero Timing Capacitance	A1, A2 to Q, $\overline{Q}$	C_{EXT} = 0 pF, R_{INT} to V_{CC}, R_L = 400Ω, C_L = 15 pF		50	ns
$t_{W(OUT)}$	Output Pulse Width Using External Timing Resistor	A1, A2 to Q, $\overline{Q}$	C_{EXT} = 100 pF, R_{INT} = 10 kΩ, R_L = 400Ω, C_L = 15 pF	600	800	ns
		A1, A2 to Q, $\overline{Q}$	C_{EXT} = 1 μF, R_{INT} = 10 kΩ, R_L = 400Ω, C_L = 15 pF	6	8	ms

Operating Rules

1. To use the internal 2 kΩ timing resistor, connect the R_{INT} pin to V_{CC}.
2. An external resistor (R_X) or the internal resistor (2 kΩ) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants use high-quality mica, glass, polypropylene, polycarbonate, or polystyrene capacitors. For large time constants use solid tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
3. The pulse width is essentially determined by external timing components R_X and C_X. For C_X < 1000 pF see *Figure 1* design curves on T_W as function of timing components value. For C_X >1000 pF the output is defined as:

   $t_W = K R_X C_X$

   where [R_X is in Kilo-ohm]

   [C_X is in pico Farad]

   [T_W is in nano second]

   [K ≈ 0.7]

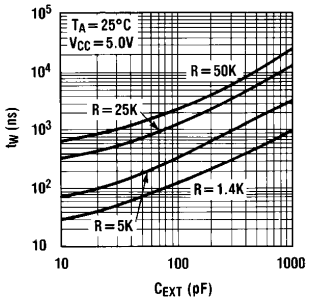


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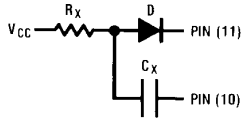
FIGURE 1

4. If C_X is an electrolytic capacitor a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current *(Figure 2)*.

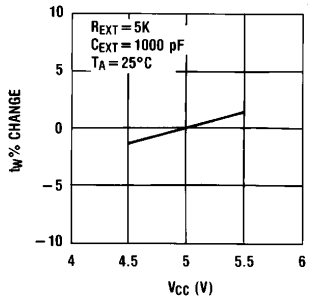


TL/F/6538–3

FIGURE 2

Operating Rules (Continued)

5. Output pulse width versus V_{CC} and operation temperatures: *Figure 3* depicts the relationship between pulse width variation versus V_{CC}. *Figure 4* depicts pulse width variation versus ambient temperature.



TL/F/6538–4

FIGURE 3

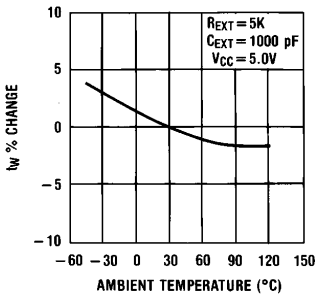


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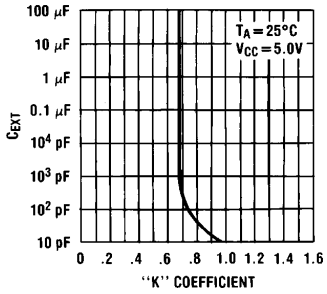
FIGURE 4

6. The "K" coefficient is not a constant, but varies as a function of the timing capacitor C_X. *Figure 5* details this characteristic.



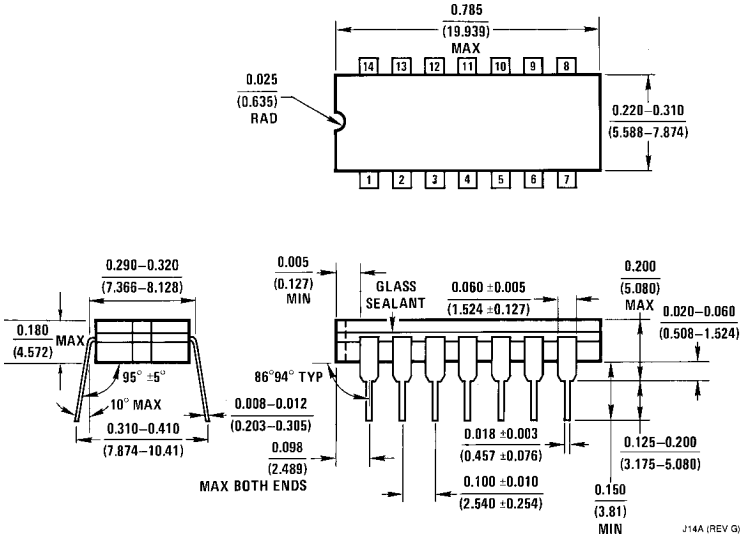
TL/F/6538–6

FIGURE 5

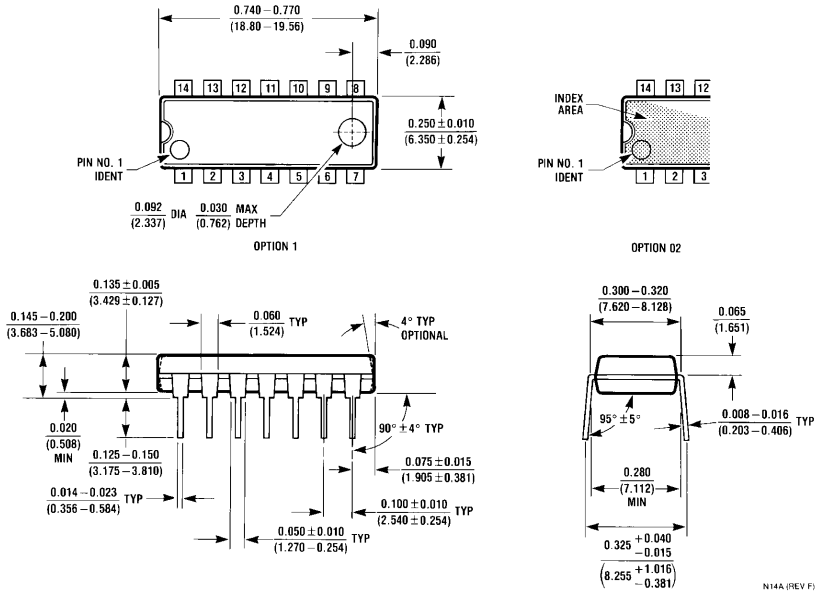
7. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I × R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (10) and (11) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
8. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC}-pin as space permits.

For further detailed device characteristics and output performance please refer to the NSC one-shot application note, AN-366.

Physical Dimensions inches (millimeters)

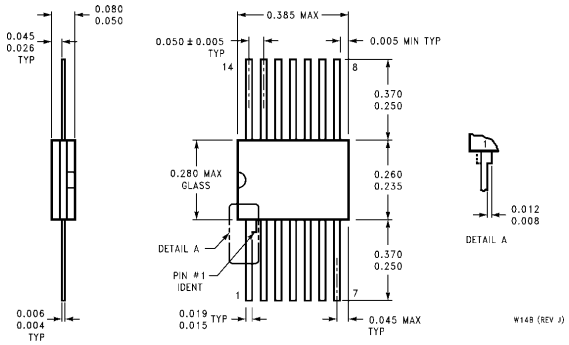


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54121DMQB or DM54121J
NS Package Number J14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74121N
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54121FMQB or DM54121W
NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

March 1998

DM7474
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

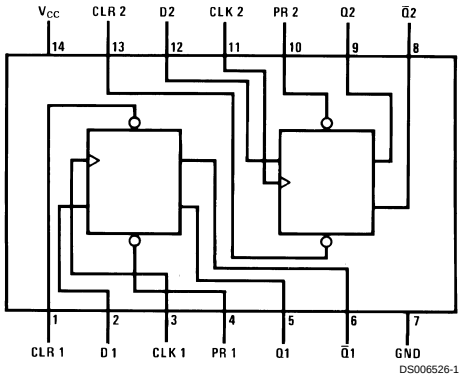
This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (5474) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 5474DMQB, 5474FMQB, DM5474J, DM5474W, DM7474M or DM7474N
See Package Number J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
PR	**CLR**	**CLK**	**D**	**Q**	$\overline{\mathbf{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
↑ = Positive-going transition of the clock.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

Q_0 = The output logic level of Q before the indicated input conditions were established.

Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55˚C to +125˚C
DM74	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		DM5474			DM7474			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0		15	0		15	MHz
t_W	Pulse Width (Note 4)	Clock High	30			30			ns
		Clock Low	37			37			
		Clear Low	30			30			
		Preset Low	30			30			
t_{SU}	Input Setup Time (Notes 3, 4)		20↑			20↑			ns
t_H	Input Hold Time (Notes 3, 4)		5↑			5↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	˚C

Note 2: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 3: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 4: T_A = 25˚C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	D			40	µA
			Clock			80	
			Clear			120	
			Preset			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V (Note 8)	D			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
			Preset			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 7)			17	30	mA

Note 5: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 6: Not more than one output should be shorted at a time.

Note 7: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

Electrical Characteristics (Continued)

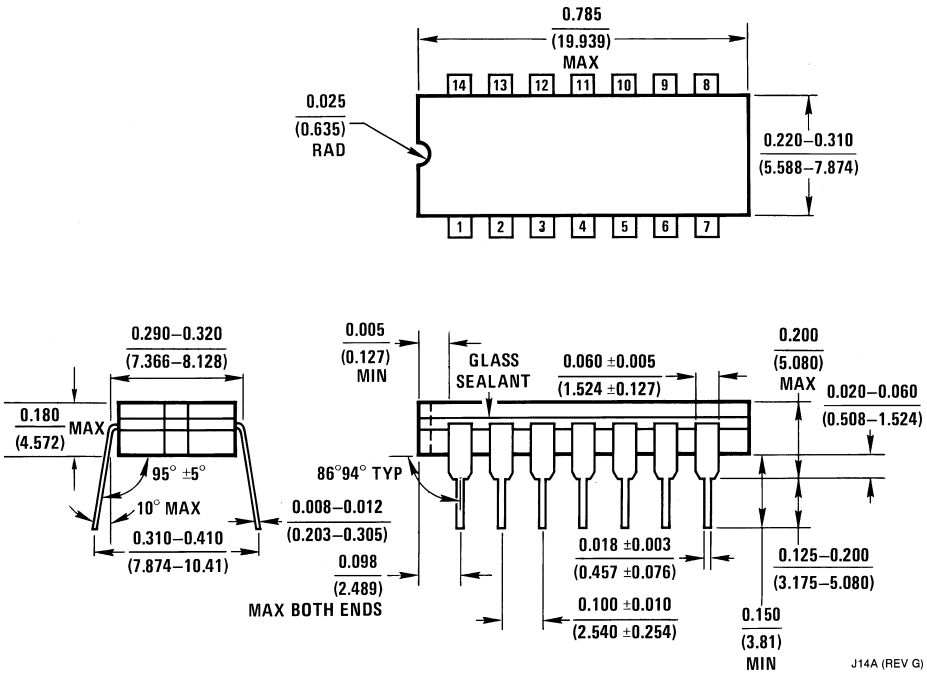
Note 8: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics

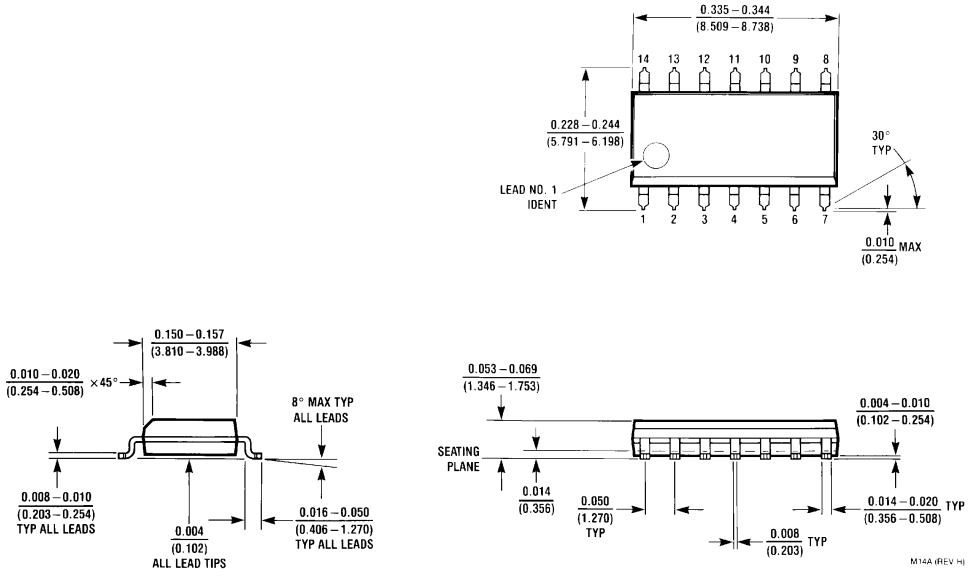
at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25	ns

Physical Dimensions inches (millimeters) unless otherwise noted

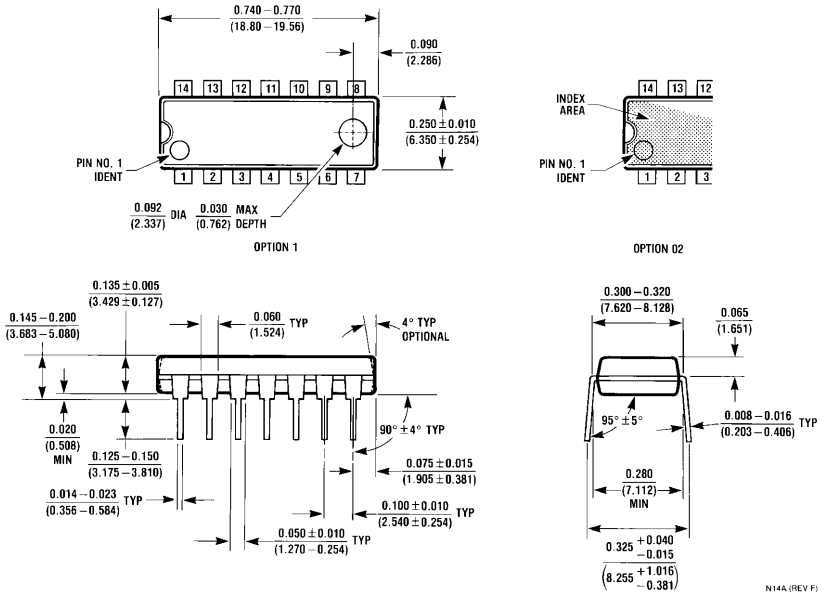


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 5474DMQB or DM5474J
Package Number J14A

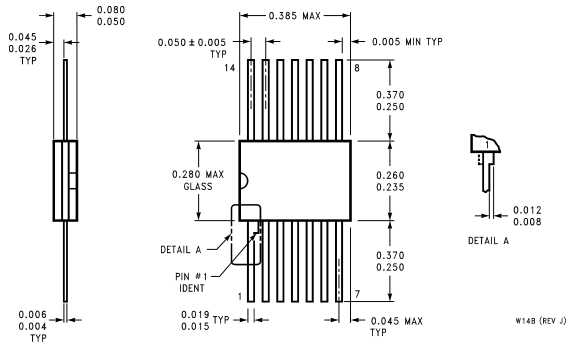


14-Lead Small Outline Molded Package (M)
Order Number DM7474M
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM7474N
Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number 5474FMQB or DM5474W
Package Number W14B

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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March 1998

FAIRCHILD SEMICONDUCTOR™

DM74LS112A
Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

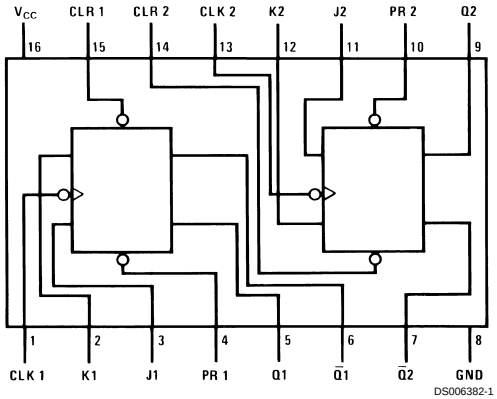
This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the falling edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as the setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (54LS112) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



DS006382-1

Order Number 54LS112DMQB, 54LS112FMQB, 54LS112LMQB, DM54LS112AJ, DM54LS112AW, DM74LS112AM or DM74LS112AN
See Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs					Outputs	
PR	**CLR**	**CLK**	**J**	**K**	**Q**	$\overline{\mathbf{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
↓ = Negative Going Edge of Pulse
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Note 1: This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.

Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		DM54LS112A			DM74LS112A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 4)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 5)		0		25	0		25	MHz
t_W	Pulse Width (Note 4)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 5)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 3, 4)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 3, 5)		25↓			25↓			ns
t_H	Hold Time (Notes 3, 4)		0↓			0↓			ns
t_H	Hold Time (Notes 3, 5)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	˚C

Note 2: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 3: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 4: C_L = 15 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 5: C_L = 50 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Preset			0.3	
			Clock			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	µA
			Clear			60	
			Preset			60	
			Clock			80	

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Preset			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 7)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 8)			4	6	mA

Switching Characteristics

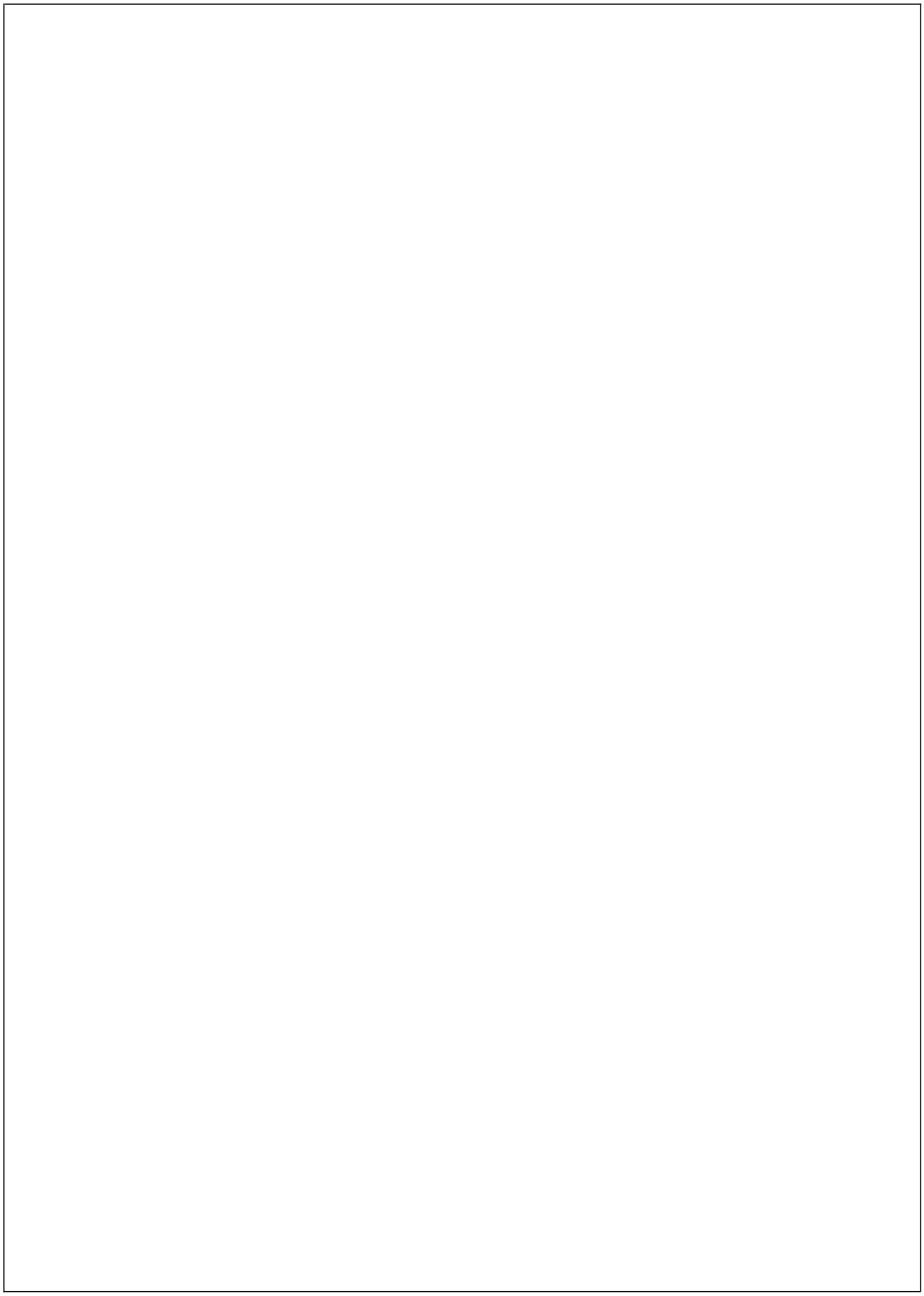
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		20		28	ns

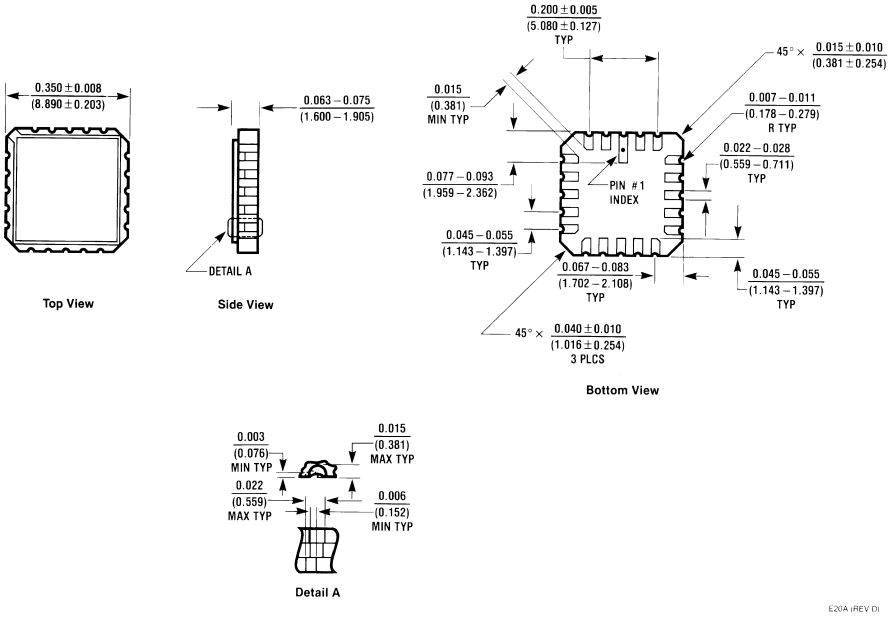
Note 6: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

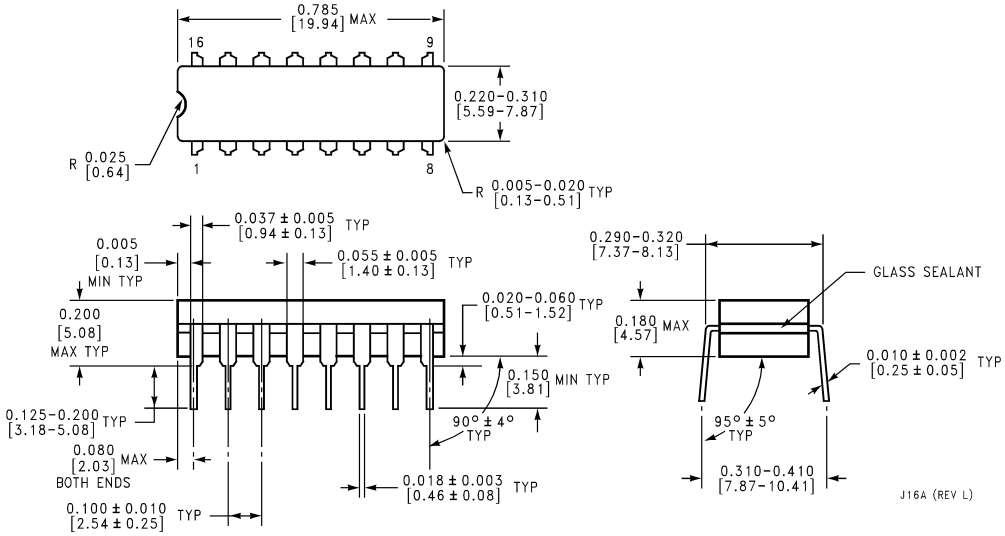
Note 8: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.



Physical Dimensions inches (millimeters) unless otherwise noted

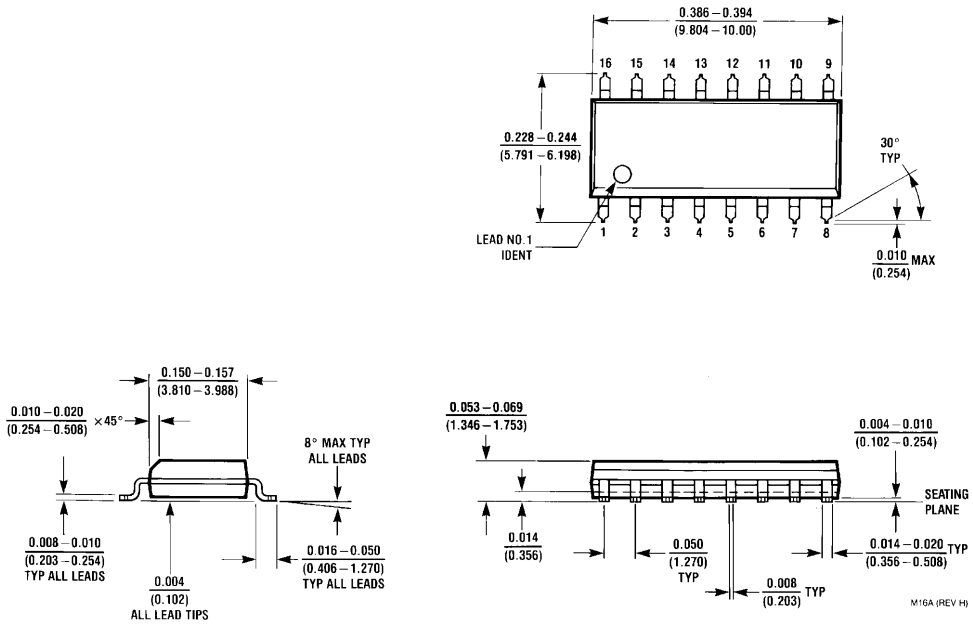


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS112LMQB
Package Number E20A

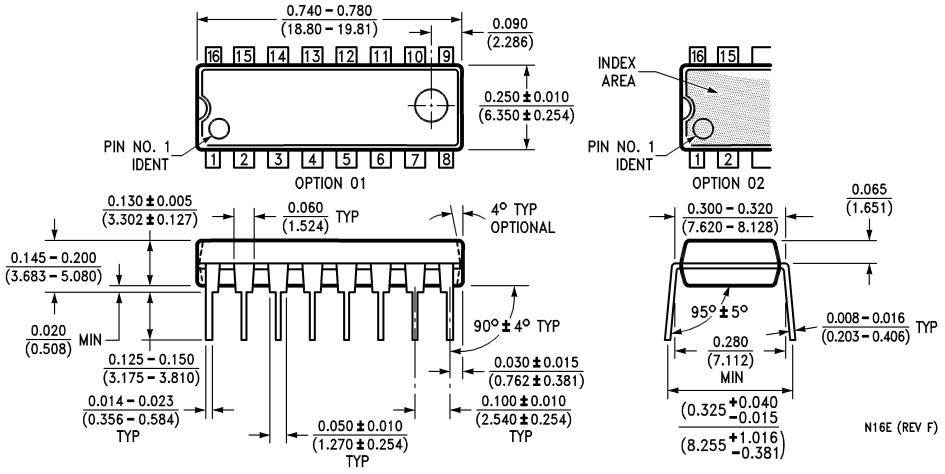


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS112DMQB or DM54LS112AJ
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

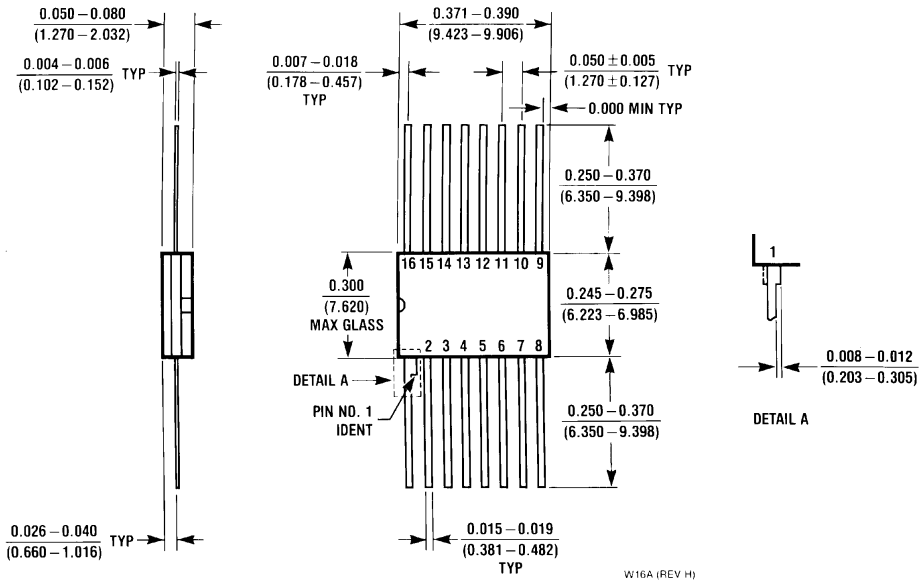


16-Lead Small Outline Molded Package (M)
Order Number DM74LS112AM
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS112AN
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS112FMQB or DM54LS112AW
Package Number W16A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

March 1998

DM74LS373/DM74LS374 3-STATE Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the DM54/74LS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

The eight flip-flops of the DM54/74LS374 are edge-triggered D-type flip flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

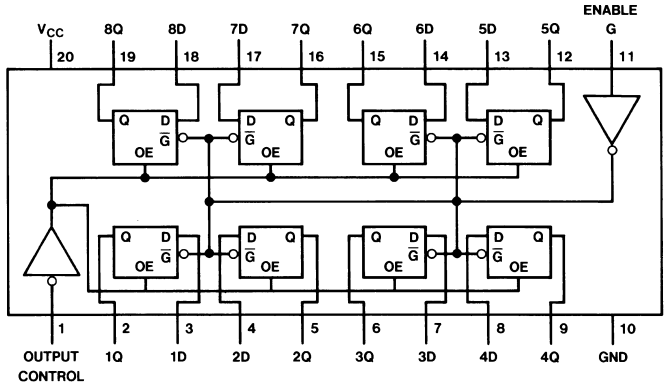
The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Choice of 8 latches or 8 D-type flip-flops in a single package
- 3-STATE bus-driving outputs
- Full parallel-access for loading
- Buffered control inputs
- P-N-P inputs reduce D-C loading on data lines

Connection Diagrams

Dual-In-Line Packages
'LS373

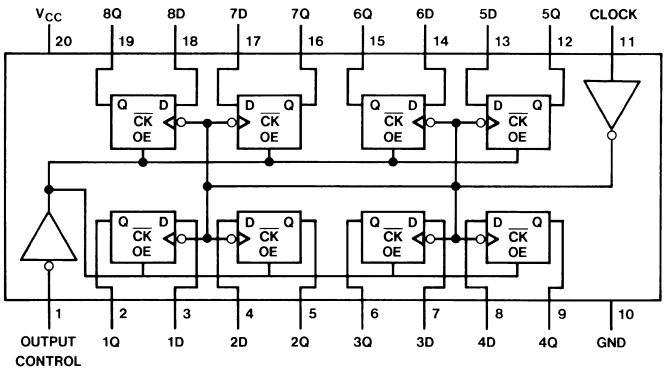


DS006431-1

Order Number DM54LS373J, DM54LS373W, DM74LS373N or DM74LS373WM
See Package Number J20A, M20B, N20A or W20A

Connection Diagrams (Continued)

'LS374



DS006431-2

Order Number DM54LS374J, DM54LS374W, DM74LS374WM or DM74LS374N
See Package Number J20A, M20B, N20A or W20A

Function Tables

DM54/74LS373

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

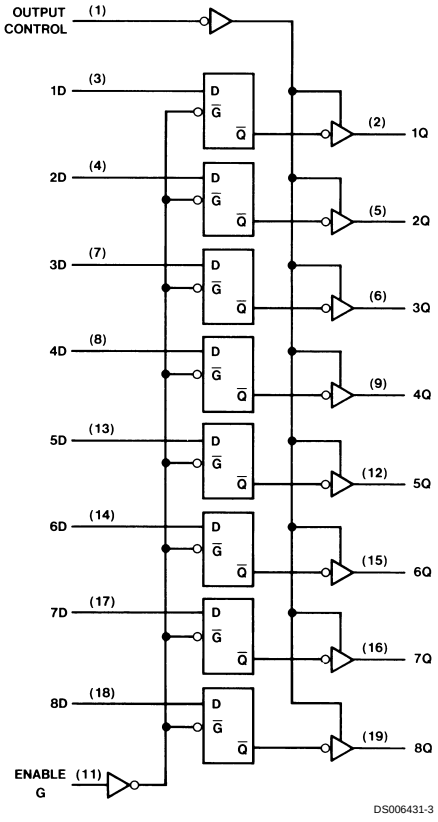
H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care
↑ = Transition from low-to-high level, Z = High Impedance State
Q_0 = The level of the output before steady-state input conditions were established.

DM54/74LS374

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

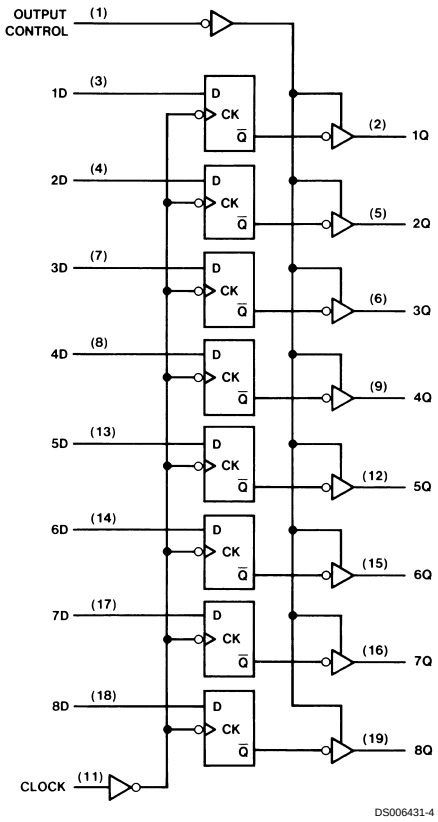
Logic Diagrams

DM54/74LS334
Transparent Latches



DS006431-3

DM54/74LS374
Positive-Edge-Triggered Flip-Flops



DS006431-4

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65˚C to +150˚C
Operating Free Air Temperature Range	
DM54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C

Recommended Operating Conditions

Symbol	Parameter		DM54LS373			DM74LS373			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Votage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
t_W	Pulse Width	Enable High	15			15			ns
	(Note 3)	Enable Low	15			15			
t_{SU}	Data Setup Time (Notes 2, 3)		5↓			5↓			ns
t_H	Data Hold Time (Notes 2, 3)		20↓			20↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 3: T_A = 25˚C and V_{CC} = 5V.

'LS373 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−50		−225	

'LS373 Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
I_{CC}	Supply Current	V_{CC} = Max, OC = 4.5V, D_n, Enable = GND		24	40	mA

'LS373 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Q		18		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Q		18		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Q		30		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Q		30		36	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Any Q		28		36	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Any Q		36		50	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)	Output Control to Any Q		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)	Output Control to Any Q		25			ns

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: C_L = 5 pF.

Recommended Operating Conditions

Symbol	Parameter	DM54LS374			DM74LS374			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA

Recommended Operating Conditions (Continued)

Symbol	Parameter		DM54LS374			DM74LS374			Units
			Min	Nom	Max	Min	Nom	Max	
t_W	Pulse Width	Clock High	15			15			ns
	(Note 8)	Clock Low	15			15			
t_{SU}	Data Setup Time (Notes 7, 8)		20↑			20↑			ns
t_H	Data Hold Time (Notes 7, 8)		1↑			1↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 7: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 8: $T_A = 25°C$ and $V_{CC} = 5V$.

'LS374 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 9)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	DM54	2.4	3.4		V
		I_{OH} = Max	DM74	2.4	3.1		
		V_{IL} = Max					
		V_{IH} = Min					
V_{OL}	Low Level Output Voltage	V_{CC} = Min	DM54		0.25	0.4	V
		I_{OL} = Max	DM74		0.35	0.5	
		V_{IL} = Max					
		V_{IH} = Min					
		I_{OL} = 12 mA	DM74		0.25	0.4	
		V_{CC} = Min					
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−50		−225	mA
		(Note 10)	DM74	−50		−225	
I_{CC}	Supply Current	V_{CC} = Max, D_n = GND, OC = 4.5V			27	45	mA

'LS374 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

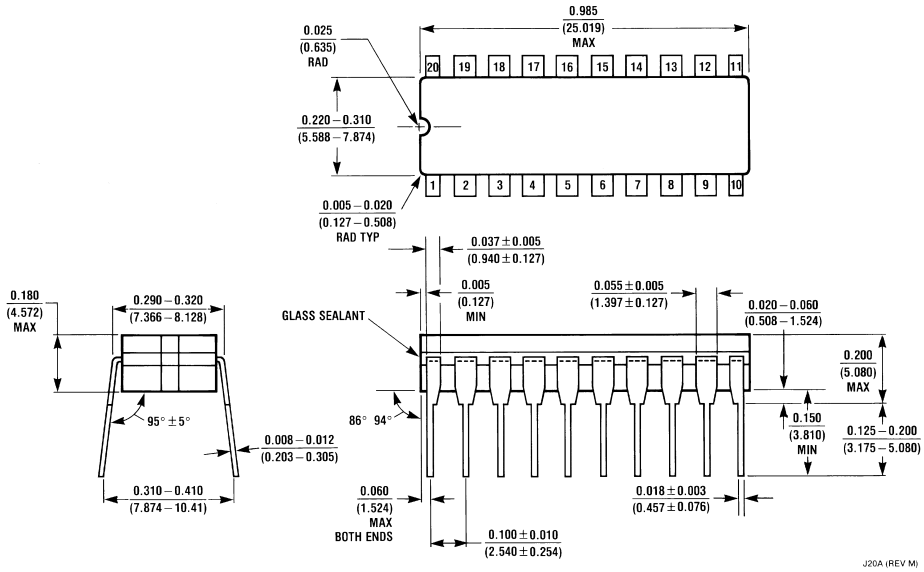
Symbol	Parameter	R_L = 667Ω				Units
		C_L = 45 pF		C_L = 150 pF		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	35		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		28		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		28		38	ns
t_{PZH}	Output Enable Time to High Level Output		28		44	ns
t_{PZL}	Output Enable Time to Low Level Output		28		44	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 11)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 11)		25			ns

Note 9: All typicals are at V_{CC} = 5V, T_A = 25˚C.

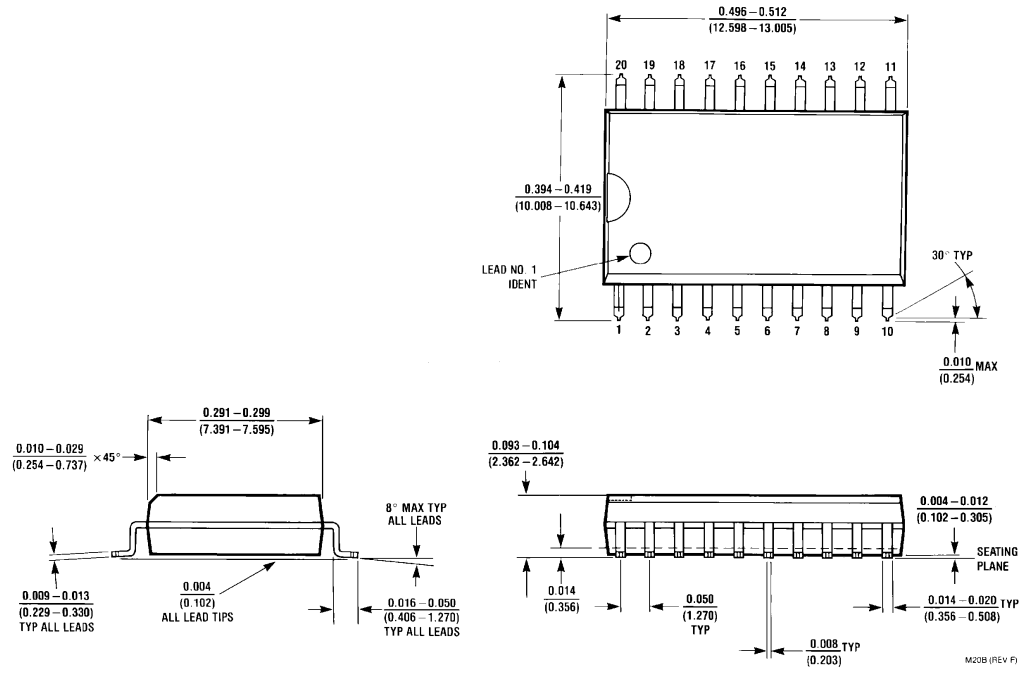
Note 10: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 11: C_L = 5 pF.

Physical Dimensions inches (millimeters) unless otherwise noted

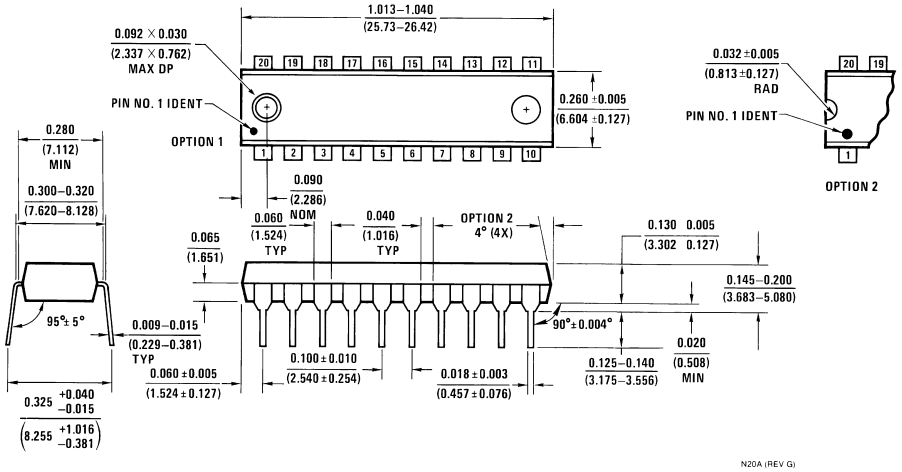


20-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS373J or DM54LS374J
Package Number J20A

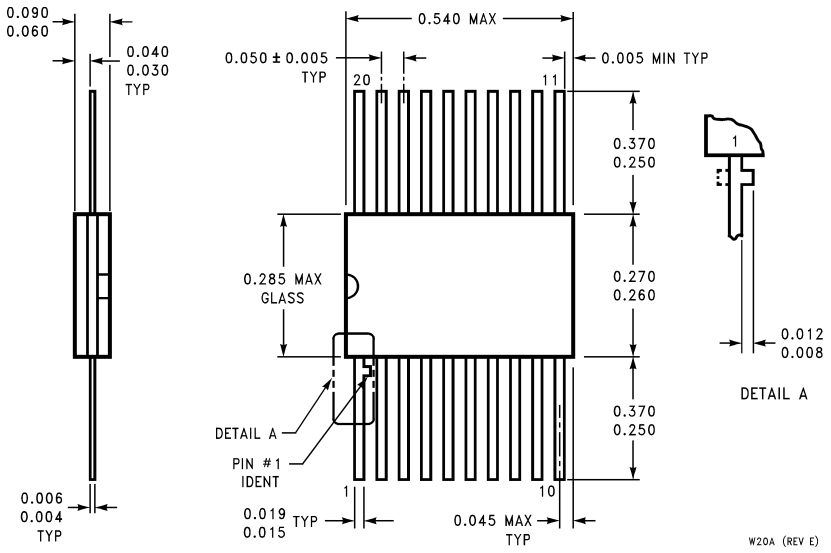


20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS373WM or DM74LS374WM
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS373N and DM74LS374N
Package Number N20A



20-Lead Ceramic Flat Package (W)
Order Number DM54LS373W or DM54LS374W
Package Number W20A

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May 1997

National Semiconductor

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

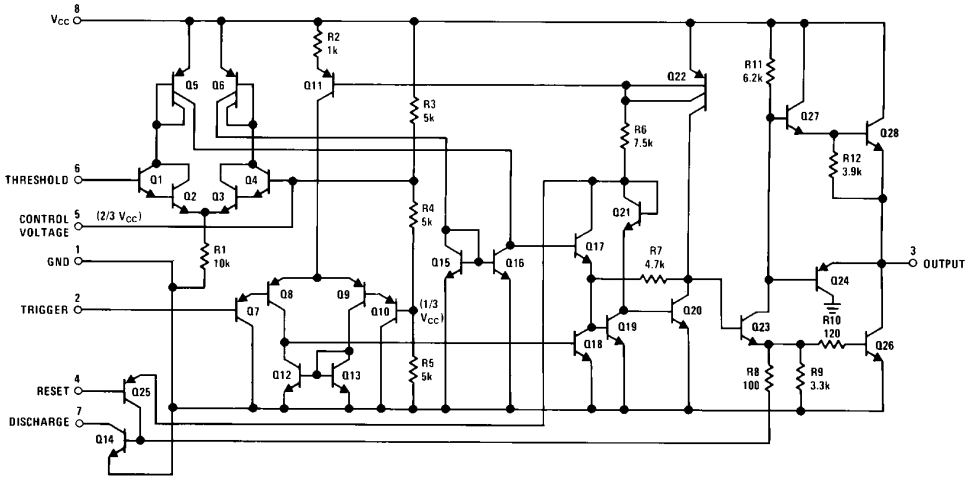
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per ˚C
- Normally on and normally off output
- Available in 8 pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



DS007851-1

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555H, LM555CH	760 mW
LM555, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0˚C to +70˚C
LM555	−55˚C to + 125˚C
Storage Temperature Range	−65˚C to +150˚C
Soldering Information	
Dual-In-Line Package	
Soldering (10 Seconds)	260˚C
Small Outline Packages	
(SOIC and MSOP)	
Vapor Phase (60 Seconds)	215˚C
Infrared (15 Seconds)	220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

(T_A = 25˚C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞		10	12		10	15	mA
	(Low State) (Note 4)							
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A = 1k to 100 kΩ,		30			50		ppm/˚C
	C = 0.1 µF, (Note 5)							
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100 kΩ,		90			150		ppm/˚C
	C = 0.1 µF, (Note 5)							
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	µA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 7)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25˚C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25˚C based on a +150˚C maximum junction temperature and a thermal resistance of 164˚C/W (T0-5), 106˚C/W (DIP), 170˚C/W (S0-8), and 204˚C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

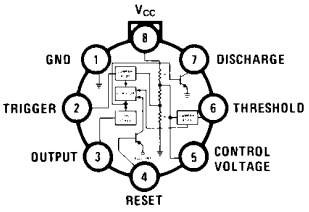
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Connection Diagrams

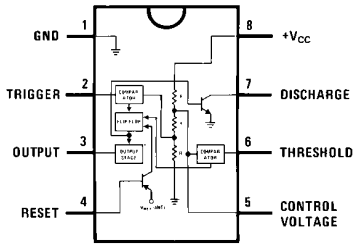
Metal Can Package



DS007851-2

Top View
Order Number LM555H or LM555CH
See NS Package Number H08C

Dual-In-Line, Small Outline and Molded Mini Small Outline Packages

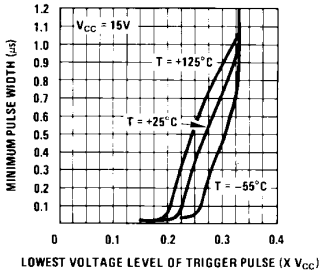


DS007851-3

Top View
Order Number LM555J, LM555CJ, LM555CM, LM555CMM or LM555CN
See NS Package Number J08A, M08A, MUA08A or N08E

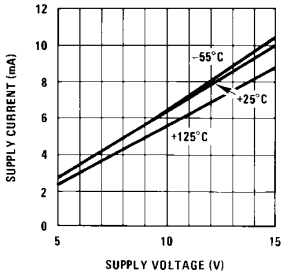
Typical Performance Characteristics

Minimuim Pulse Width Required for Triggering



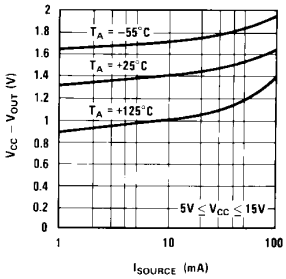
DS007851-4

Supply Current vs Supply Voltage



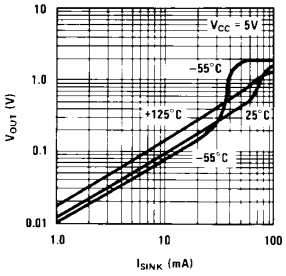
DS007851-19

High Output Voltage vs Output Source Current



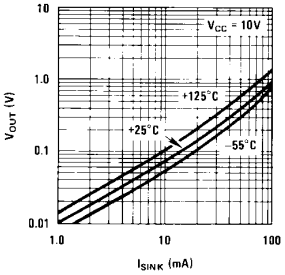
DS007851-20

Low Output Voltage vs Output Sink Current



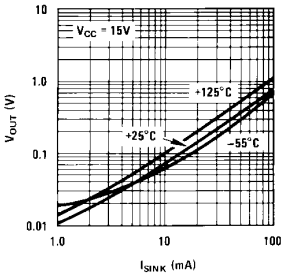
DS007851-21

Low Output Voltage vs Output Sink Current



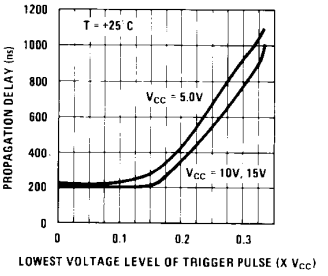
DS007851-22

Low Output Voltage vs Output Sink Current



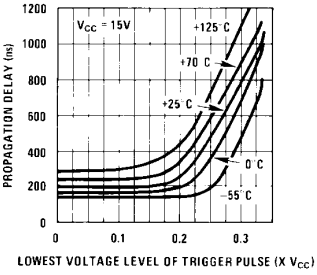
DS007851-23

Output Propagation Delay vs Voltage Level of Trigger Pulse



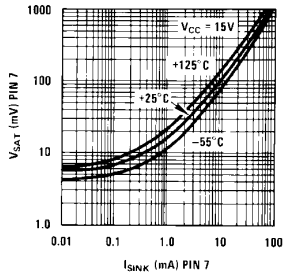
DS007851-24

Output Propagation Delay vs Voltage Level of Trigger Pulse



DS007851-25

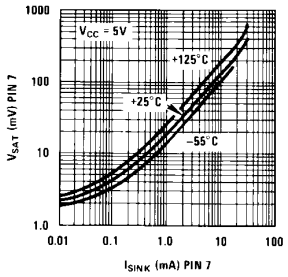
Discharge Transistor (Pin 7) Voltage vs Sink Current



DS007851-26

Typical Performance Characteristics (Continued)

Discharge Transistor (Pin 7) Voltage vs Sink Current

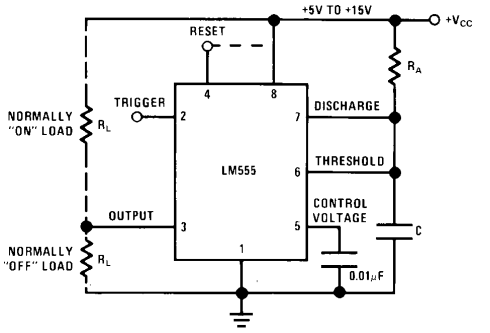


DS007851-27

Applications Information

MONOSTABLE OPERATION

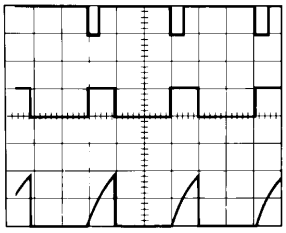
In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.



DS007851-5

FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



DS007851-6

V_{CC} = 5V Top Trace: Input 5V/Div.
TIME = 0.1 ms/DIV. Middle Trace: Output 5V/Div.
R_A = 9.1 kΩ Bottom Trace: Capacitor Voltage 2V/Div.
C = 0.01 μF

FIGURE 2. Monostable Waveforms

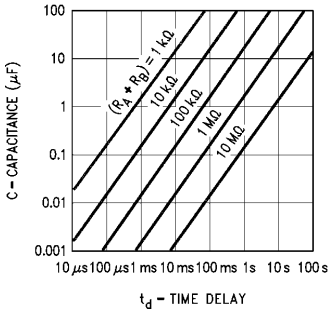
During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10 μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

Applications Information (Continued)

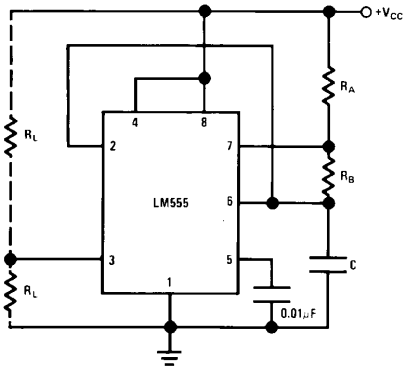


DS007851-7

FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

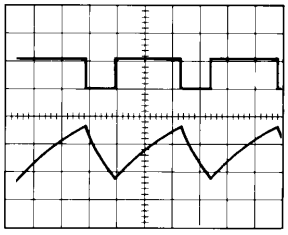


DS007851-8

FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveforms generated in this mode of operation.



DS007851-9

V_{CC} = 5V
TIME = 20 μs/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

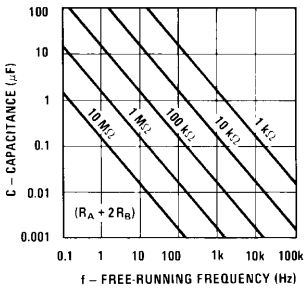
The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$



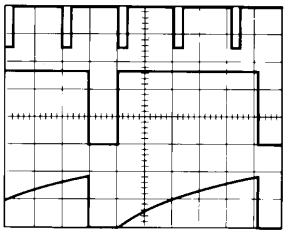
DS007851-10

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.

Applications Information (Continued)



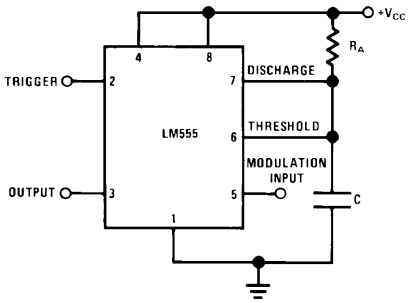
DS007851-11

V_{CC} = 5V Top Trace: Input 4V/Div.
TIME = 20 µs/DIV. Middle Trace: Output 2V/Div.
R_A = 9.1 kΩ Bottom Trace: Capacitor 2V/Div.
C = 0.01 µF

FIGURE 7. Frequency Divider

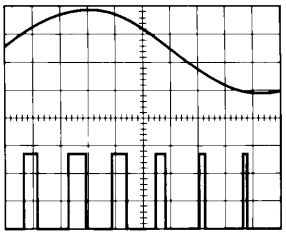
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.



DS007851-12

FIGURE 8. Pulse Width Modulator



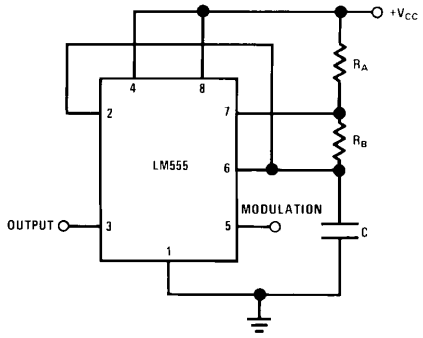
DS007851-13

V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1 kΩ
C = 0.01 µF

FIGURE 9. Pulse Width Modulator

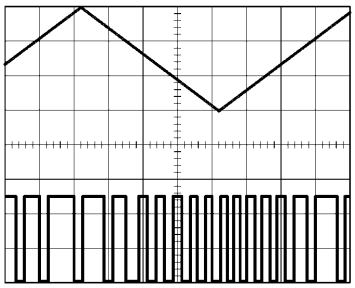
PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.



DS007851-14

FIGURE 10. Pulse Position Modulator



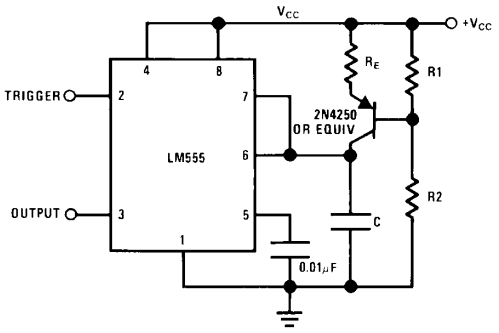
DS007851-15

V_{CC} = 5V Top Trace: Modulation Input 1V/Div.
TIME = 0.1 ms/DIV. Bottom Trace: Output 2V/Div.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 µF

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.



DS007851-16

FIGURE 12.

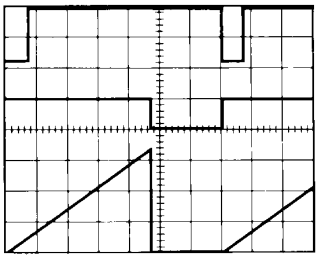
Applications Information (Continued)

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$

$$V_{BE} \cong 0.6V$$



DS007851-17

V_{CC} = 5V
TIME = 20 µs/DIV.
R_1 = 47 kΩ
R_2 = 100 kΩ
R_E = 2.7 kΩ
C = 0.01 µF

Top Trace: Input 3V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 13. Linear Ramp

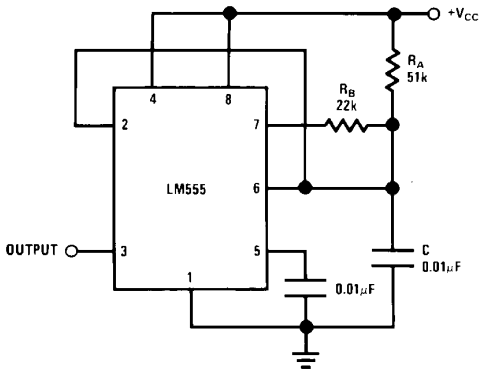
50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A\ R_B)/(R_A + R_B)\right]\ C\ \ell n\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$



DS007851-18

FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

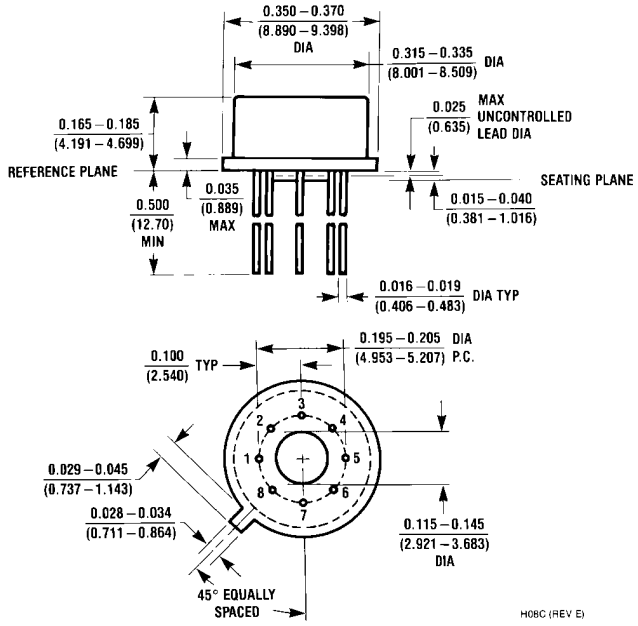
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1 µF in parallel with 1 µF electrolytic.

Lower comparator storage time can be as long as 10 µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10 µs minimum.

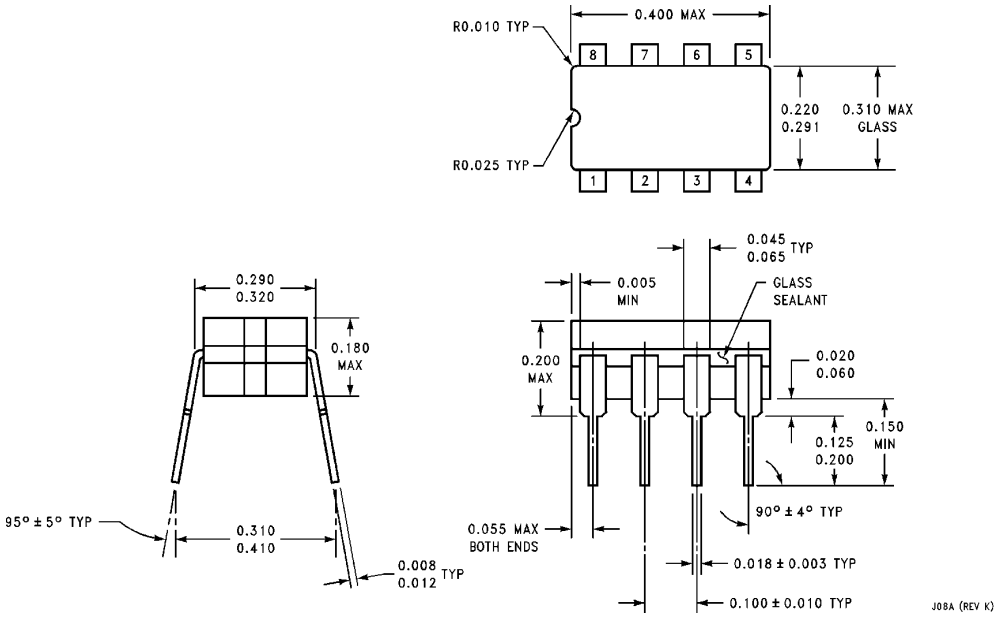
Delay time reset to output is 0.47 µs typical. Minimum reset pulse width must be 0.3 µs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

Physical Dimensions inches (millimeters)

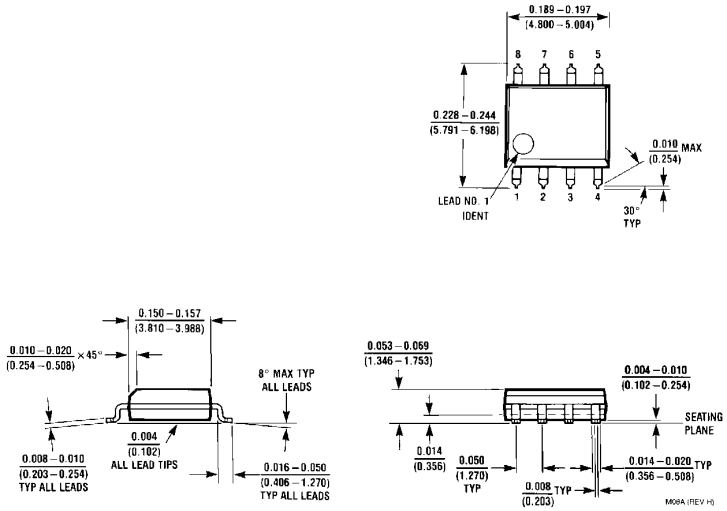


Metal Can Package (H)
Order Number LM555H or LM555CH
NS Package Number H08C



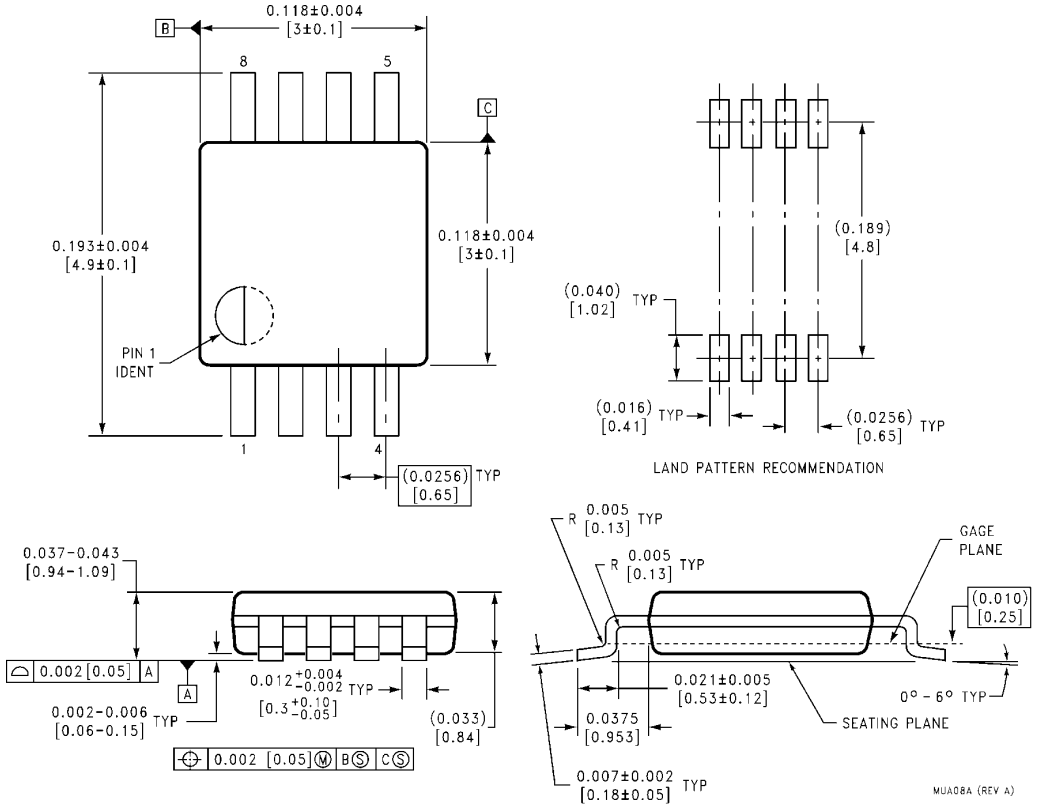
Ceramic Dual-In-Line Package (J)
Order Number LM555J or LM555CJ
NS Package Number J08A

Physical Dimensions inches (millimeters) (Continued)



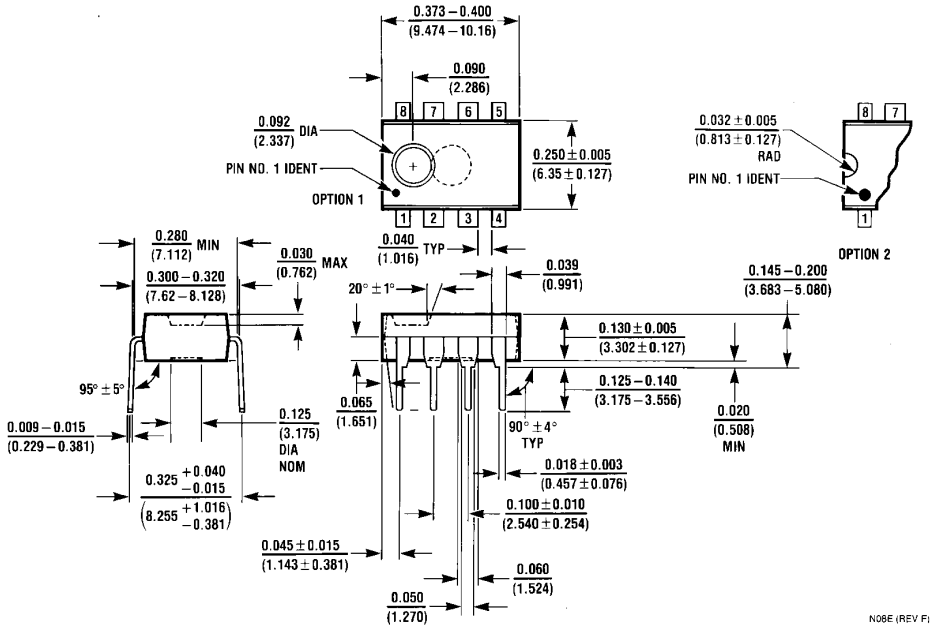
Small Outline Package (M)
Order Number LM555CM
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



8-Lead (0.118" Wide) Molded Mini Small Outline Package
Order Number LM555CMM
NS Package Number MUA08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LM555CN
NS Package Number N08E

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